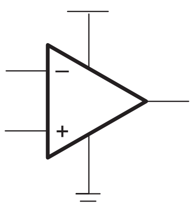
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

Check for Samples: TLC080 , TLC081, TLC082, TLC083, TLC084, TLC085, TLC08xA

FEATURES

- **Wide Bandwidth: 10 MHz**
- **High Output Drive:**
  - **I_{OH}: 57 mA at V_{DD} – 1.5 V**
  - **I_{OL}: 55 mA at 0.5 V**
- **High Slew Rate:**
  - **SR+: 16 V/μs**
  - **SR–: 19 V/μs**
- **Wide Supply Range: 4.5 V to 16 V**
- **Supply Current: 1.9 mA/Channel**
- **Ultralow Power Shutdown Mode:**
  - **I_{DD}: 125 μA/Channel**
- **Low Input Noise Voltage: 8.5 nV$\sqrt{Hz}$**
- **Input Offset Voltage: 60 μV**
- **Ultra-Small Packages:**
  - **8- or 10-Pin MSOP (TLC080/1/2/3)**



DESCRIPTION

The first members of TI's new BiMOS general-purpose operational amplifier family are the TLC08x. The BiMOS family concept is simple: provide an upgrade path for BiFET users who are moving away from dual-supply to single-supply systems and demand higher ac and dc performance. With performance rated from 4.5 V to 16 V across commercial (0°C to 70°C) and an extended industrial temperature range (–40°C to 125°C), BiMOS suits a wide range of audio, automotive, industrial, and instrumentation applications. Familiar features like offset nulling pins, and new features like MSOP PowerPAD™ packages and shutdown modes, enable higher levels of performance in a variety of applications.

Developed in TI's patented LBC3 BiCMOS process, the new BiMOS amplifiers combine a very high input impedance, low-noise CMOS front end with a high-drive bipolar output stage, thus providing the optimum performance features of both. AC performance improvements over the TL08x BiFET predecessors include a bandwidth of 10 MHz (an increase of 300%) and voltage noise of 8.5 nV/$\sqrt{Hz}$ (an improvement of 60%). DC improvements include an ensured V_{ICR} that includes ground, a factor of 4 reduction in input offset voltage down to 1.5 mV (maximum) in the standard grade, and a power supply rejection improvement of greater than 40 dB to 130 dB. Added to this list of impressive features is the ability to drive ±50-mA loads comfortably from an ultrasmall-footprint MSOP PowerPAD package, which positions the TLC08x as the ideal high-performance general-purpose operational amplifier family.

FAMILY PACKAGE TABLE

DEVICE	NO. OF CHANNELS	PACKAGE TYPES					UNIVERSAL EVM BOARD
		MSOP	PDIP	SOIC	TSSOP	SHUTDOWN	
TLC080	1	8	8	8	—	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLC081	1	8	8	8	—		
TLC082	2	8	8	8	—	—	
TLC083	2	10	14	14	—	Yes	
TLC084	4		14	14	20	—	
TLC085	4		16	16	20	Yes	

TLC080 and TLC081 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	SMALL OUTLINE (D)(1)	SMALL OUTLINE (DGN)(1)	SYMBOL	PLASTIC DIP (P)
0°C to 70°C	TLC080CD	TLC080CDGN	xxTIACW	TLC080CP
	TLC081CD	TLC081CDGN	xxTIACY	TLC081CP
–40°C to 125°C	TLC080ID	TLC080IDGN	xxTIACX	TLC080IP
	TLC081ID	TLC081IDGN	xxTIACZ	TLC081IP
	TLC080AID	—	—	TLC080AIP
	TLC081AID	—	—	TLC081AIP

(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC080CDR).

TLC082 and TLC083 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES						
	SMALL OUTLINE (D)(1)	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)
		(DGN)(1)	SYMBOL(2)	(DGQ)(1)	SYMBOL(2)		
0°C to 70°C	TLC082CD	TLC082CDGN	xxTIADZ	—	—	—	TLC082CP
	TLC083CD	—	—	TLC083CDGQ	xxTIAEB	TLC083CN	—
–40°C to 125°C	TLC082ID	TLC082IDGN	xxTIAEA	—	—	—	TLC082IP
	TLC083ID	—	—	TLC083IDGQ	xxTIAEC	TLC083IN	—
	TLC082AID	—	—	—	—	—	TLC082AIP
	TLC083AID	—	—	—	—	TLC083AIN	—

(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC082CDR).
(2) xx represents the device date code.

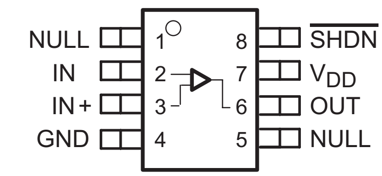
TLC084 and TLC085 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		
	SMALL OUTLINE (D)(1)	PLASTIC DIP (N)	TSSOP (PWP)(1)
0°C to 70°C	TLC084CD	TLC084CN	TLC084CPWP
	TLC085CD	TLC085CN	TLC085CPWP
–40°C to 125°C	TLC084ID	TLC084IN	TLC084IPWP
	TLC085ID	TLC085IN	TLC085IPWP
	TLC084AID	TLC084AIN	TLC084AIPWP
	TLC085AID	TLC085AIN	TLC085AIPWP

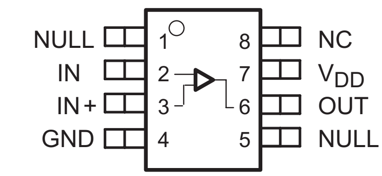
(1) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC084CDR).

For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

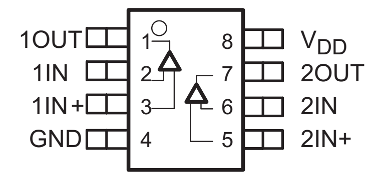
TLC080
D, DGN, OR P PACKAGE
(TOP VIEW)



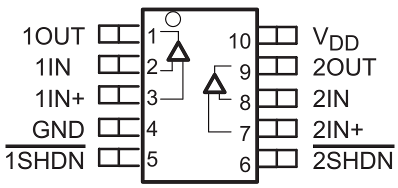
TLC081
D, DGN, OR P PACKAGE
(TOP VIEW)



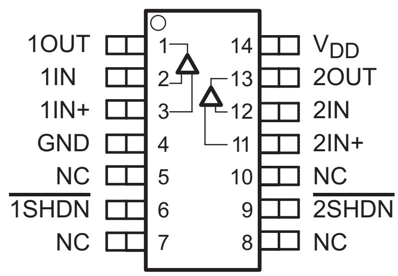
TLC082
D, DGN, OR P PACKAGE
(TOP VIEW)



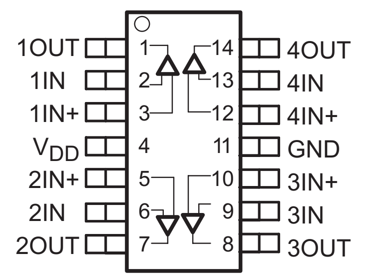
TLC083
DGQ PACKAGE
(TOP VIEW)



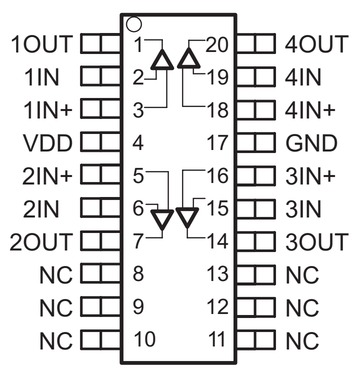
TLC083
D OR N PACKAGE
(TOP VIEW)



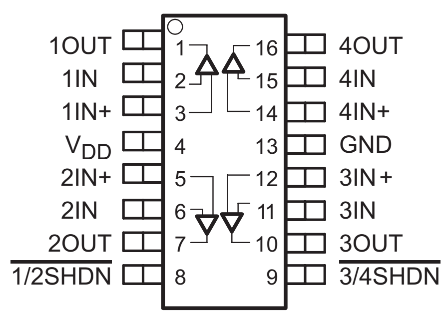
TLC084
D OR N PACKAGE
(TOP VIEW)



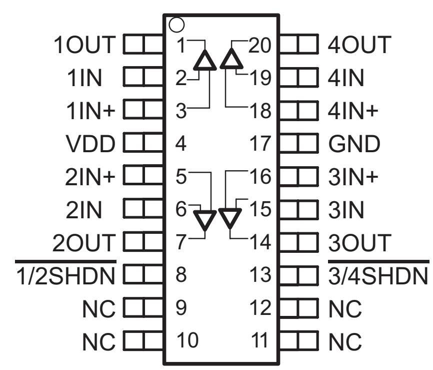
TLC084
PWP PACKAGE
(TOP VIEW)



TLC085
D OR N PACKAGE
(TOP VIEW)

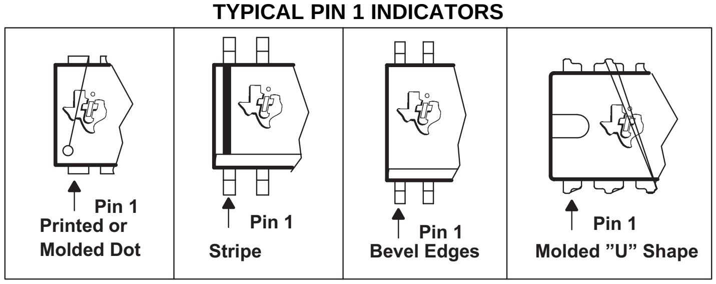


TLC085
PWP PACKAGE
(TOP VIEW)



NC - No internal connection

TYPICAL PIN 1 INDICATORS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		VALUE	UNIT
Supply voltage, V_{DD} [2]		17	V
Differential input voltage range, V_{ID}		±VDD	
Continuous total power dissipation		See Dissipation Rating Table	
Operating free-air temperature range, T_A:	C suffix	0 to 70	°C
	I suffix	−40 to 125	°C
Maximum junction temperature, T_J		150	°C
Storage temperature range, T_{stg}		–65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND .

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DGN (8)	4.7	52.7	2.37 W
DGQ (10)	4.7	52.3	2.39 W
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PWP (20)	1.40	26.1	4.79 W

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	4.5	16	V
	Split supply	±2.25	±8	
Common-mode input voltage, V_{ICR}		GND	V_{DD}–2	V
Shutdown on/off voltage level[1]	V_{IH}	2		V
	V_{IL}		0.8	
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	–40	125	

(1) Relative to the voltage on the GND terminal of the device.

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TA(1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω	TLC080/1/2/3, TLC084/5	25°C		390	1900	µV
				Full range			3000	
			TLC080/1/2/3A, TLC084/5A	25°C		390	1400	
				Full range			2000	
$\propto V_{IO}$	Temperature coefficient of input offset voltage					1.2		µV/°C
I_{IO}	Input offset current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C		1.9	50	pA
			TLC08XC	Full range			100	
			TLC08XI				700	
I_{IB}	Input bias current			25°C		3	50	pA
			TLC08XC	Full range			100	
			TLC08XI				700	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω		25°C	0 to 3.0	0 to 3.5		V
				Full range	0 to 3.0	0 to 3.5		
V_{OH}	High-level output voltage	V_{IC} = 2.5 V	I_{OH} = –1 mA	25°C	4.1	4.3		V
				Full range	3.9			
			I_{OH} = –20 mA	25°C	3.7	4		
				Full range	3.5			
			I_{OH} = –35 mA	25°C	3.4	3.8		
				Full range	3.2			
			I_{OH} = –50 mA	25°C	3.2	3.6		
				–40°C to 85°C	3			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 1 mA	25°C		0.18	0.25	V
				Full range			0.35	
			I_{OL} = 20 mA	25°C		0.35	0.39	
				Full range			0.45	
			I_{OL} = 35 mA	25°C		0.43	0.55	
				Full range			0.7	
			I_{OL} = 50 mA	25°C		0.45	0.63	
				–40°C to 85°C			0.7	
I_{OS}	Short-circuit output current	Sourcing		25°C		100		mA
		Sinking		25°C		100		
I_O	Output current	V_{OH} = 1.5 V from positive rail		25°C		57		mA
		V_{OL} = 0.5 V from negative rail		25°C		55		
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 3 V,	R_L = 10 kΩ	25°C	100	120		dB
				Full range	100			
$r_{i(d)}$	Differential input resistance			25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		22.9		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		0.25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3 V,	R_S = 50 Ω	25°C	80	110		dB
				Full range	80			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 4.5 V to 16 V, No load	V_{IC} = V_{DD}/2,	25°C	80	100		dB
				Full range	80			

(1) Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

ELECTRICAL CHARACTERISTICS (continued)

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TA(1)	MIN	TYP	MAX	UNIT
I_{DD}	Supply current (per channel)	V_O = 2.5 V,	No load	25°C		1.8	2.5	mA
				Full range			3.5	
$I_{DD(SHDN)}$	Supply current in shutdown mode (per channel) (TLC080, TLC083, TLC085)	$\overline{SHDN}$ ≤ 0.8 V		25°C		125	200	µA
				Full range			250	

OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A(1)	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 50 pF,	25°C	10	16		V/µs
				Full range	9.5			
SR–	Negative slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 50 pF,	25°C	12.5	19		V/µs
				Full range	10			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		12		nV/√Hz
		f = 1 kHz		25°C		8.5		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA /√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 3 V,	A_V = 1	25°C		0.002		%
		R_L = 10 kΩ and 250 Ω,	A_V = 10			0.012		
		f = 1 kHz	A_V = 100			0.085		
$t_{(on)}$	Amplifier turnon time(2)	R_L = 10 kΩ		25°C		0.15		µs
$t_{(off)}$	Amplifier turnoff time(2)			25°C		1.3		µs
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		10		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 1 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		0.18		µs
			0.01%			0.39		
		$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 47 pF, R_L = 10 kΩ	0.1%			0.18		
			0.01%			0.39		
$φ_m$	Phase margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		32		°
		R_L = 10 kΩ,	C_L = 0 pF			40		
	Gain margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		2.2		dB
		R_L = 10 kΩ,	C_L = 0 pF			3.3		

(1) Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.
(2) Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TA(1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 12 V, V_{IC} = 6 V, V_O = 6 V, R_S = 50 Ω	TLC080/1/2/3, TLC084/5	25°C		390	1900	μV
				Full range			3000	
			TLC080/1/2/3A, TLC084/5A	25°C		390	1400	
				Full range			2000	
αV_{IO}	Temperature coefficient of input offset voltage					1.2		μV/°C
I_{IO}	Input offset current	V_{DD} = 12 V, V_{IC} = 6 V, V_O = 6 V, R_S = 50 Ω		25°C		1.5	50	pA
			TLC08xC	Full range			100	
			TLC08xI				700	
I_{IB}	Input bias current			25°C		3	50	pA
			TLC08xC	Full range			100	
			TLC08xI				700	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω		25°C	0 to 10.0	0 to 10.5		V
				Full range	0 to 10.0	0 to 10.5		
V_{OH}	High-level output voltage	V_{IC} = 6 V	I_{OH} = –1 mA	25°C	11.1	11.2		V
				Full range	11			
			I_{OH} = –20 mA	25°C	10.8	11		
				Full range	10.7			
			I_{OH} = –35 mA	25°C	10.6	10.7		
				Full range	10.3			
			I_{OH} = –50 mA	25°C	10.3	10.5		
				–40°C to 85°C	10.2			
V_{OL}	Low-level output voltage	V_{IC} = 6 V	I_{OL} = 1 mA	25°C		0.17	0.25	V
				Full range			0.35	
			I_{OL} = 20 mA	25°C		0.35	0.45	
				Full range			0.5	
			I_{OL} = 35 mA	25°C		0.4	0.52	
				Full range			0.6	
			I_{OL} = 50 mA	25°C		0.45	0.6	
				–40°C to 85°C			0.65	
I_{OS}	Short-circuit output current	Sourcing		25°C		150		mA
		Sinking		25°C		150		
I_O	Output current	V_{OH} = 1.5 V from positive rail		25°C		57		mA
		V_{OL} = 0.5 V from negative rail		25°C		55		
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 8 V,	R_L = 10 kΩ	25°C	120	140		dB
				Full range	120			
$r_{i(d)}$	Differential input resistance			25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		21.6		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		0.25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 10 V,	R_S = 50 Ω	25°C	80	110		dB
				Full range	80			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 4.5 V to 16 V, No load	V_{IC} = V_{DD}/2,	25°C	80	100		dB
				Full range	80			

(1) Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

ELECTRICAL CHARACTERISTICS (continued)

at specified free-air temperature, V_{DD} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TA[(1)]	MIN	TYP	MAX	UNIT
I_{DD}	Supply current (per channel)	V_O = 7.5 V,	No load	25°C		1.9	2.9	mA
				Full range			3.5	
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLC080, TLC083, TLC085) (per channel)	$\overline{SHDN}$ ≤ 0.8 V		25°C		125	200	μA
				Full range			250	

OPERATING CHARACTERISTICS

at specified free-air temperature, V_{DD} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A[(1)]	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 50 pF,	25°C	10	16		V/μs
				Full range	9.5			
SR–	Negative slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 50 pF,	25°C	12.5	19		V/μs
				Full range	10			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		14		nV/√Hz
		f = 1 kHz		25°C		8.5		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA /√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 8 V, R_L = 10 kΩ and 250 Ω, f = 1 kHz	A_V = 1	25°C		0.002		%
			A_V = 10			0.005		
			A_V = 100			0.022		
$t_{(on)}$	Amplifier turnon time[(2)]	R_L = 10 kΩ		25°C		0.47		μs
$t_{(off)}$	Amplifier turnoff time[(2)]			25°C		2.5		μs
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		10		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 1 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		0.17		μs
			0.01%			0.22		
		$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 47 pF, R_L = 10 kΩ	0.1%			0.17		
			0.01%			0.29		
$φ_m$	Phase margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		37		°
		R_L = 10 kΩ,	C_L = 0 pF			42		
	Gain margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		3.1		dB
		R_L = 10 kΩ,	C_L = 0 pF			4		

(1) Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.
(2) Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IO}	Input offset current	vs Free-air temperature	3, 4
I_{IB}	Input bias current	vs Free-air temperature	3, 4
V_{OH}	High-level output voltage	vs High-level output current	5, 7
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8
Z_o	Output impedance	vs Frequency	9
I_{DD}	Supply current	vs Supply voltage	10
PSRR	Power supply rejection ratio	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
V_n	Equivalent input noise voltage	vs Frequency	13
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	14, 15
	Crosstalk	vs Frequency	16
	Differential voltage gain	vs Frequency	17, 18
	Phase	vs Frequency	17, 18
φ_m	Phase margin	vs Load capacitance	19, 20
	Gain margin	vs Load capacitance	21, 22
	Gain-bandwidth product	vs Supply voltage	23
SR	Slew rate	vs Supply voltage vs Free-air temperature	24 25, 26
THD + N	Total harmonic distortion plus noise	vs Frequency	27, 28
		vs Peak-to-peak output voltage	29, 30
	Large-signal follower pulse response		31, 32
	Small-signal follower pulse response		33
	Large-signal inverting pulse response		34, 35
	Small-signal inverting pulse response		36
	Shutdown forward isolation	vs Frequency	37, 38
	Shutdown reverse isolation	vs Frequency	39, 40
	Shutdown supply current	vs Supply voltage	41
		vs Free-air temperature	42
	Shutdown pulse		43, 44

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

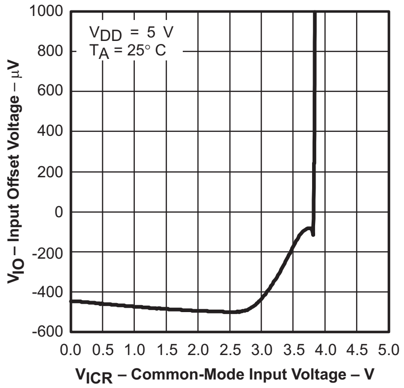


Figure 1.

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

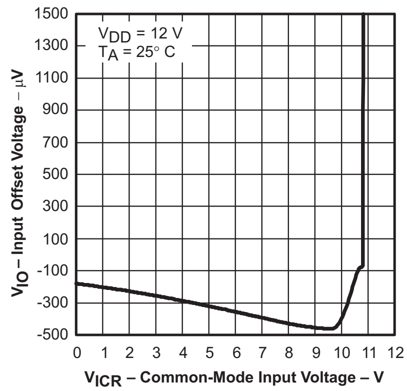


Figure 2.

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

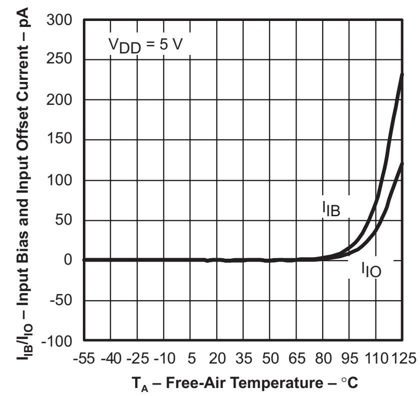


Figure 3.

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

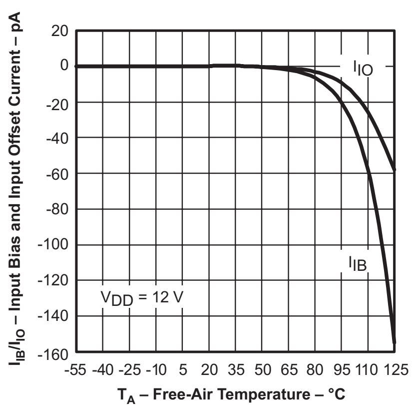


Figure 4.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

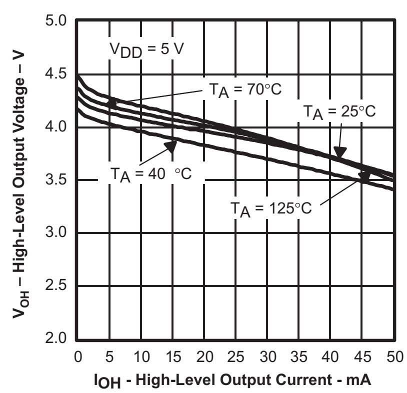


Figure 5.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

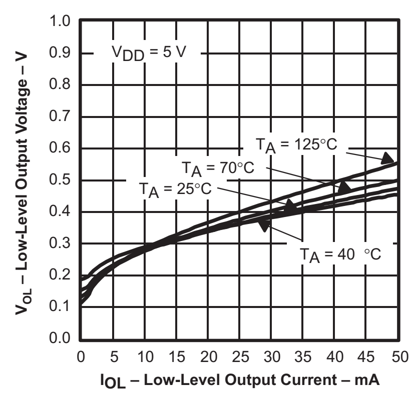


Figure 6.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

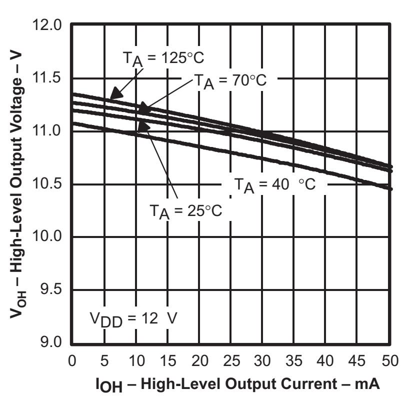


Figure 7.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

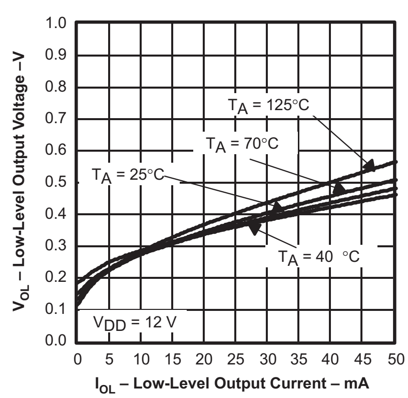


Figure 8.

OUTPUT IMPEDANCE vs FREQUENCY

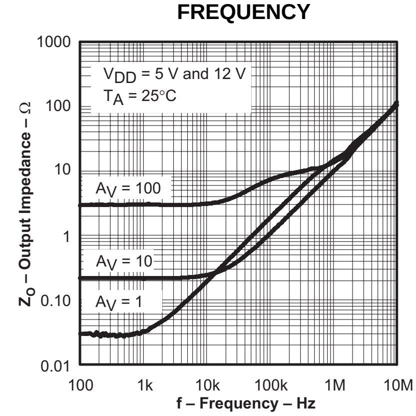


Figure 9.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

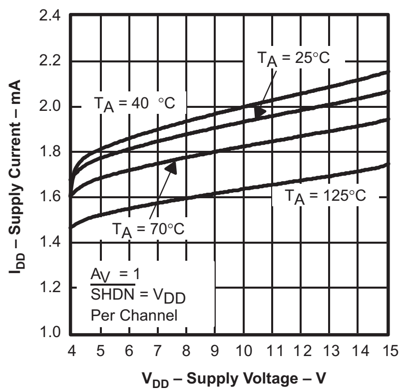


Figure 10.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

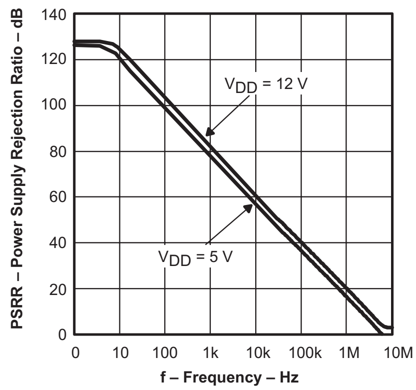


Figure 11.

COMMON-MODE REJECTION RATIO vs FREQUENCY

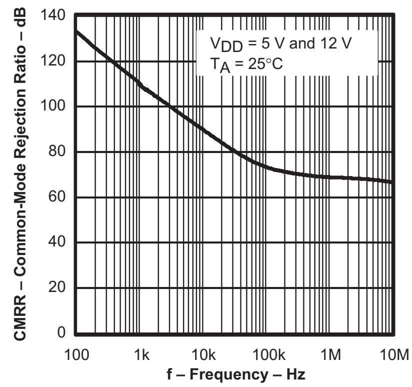


Figure 12.

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

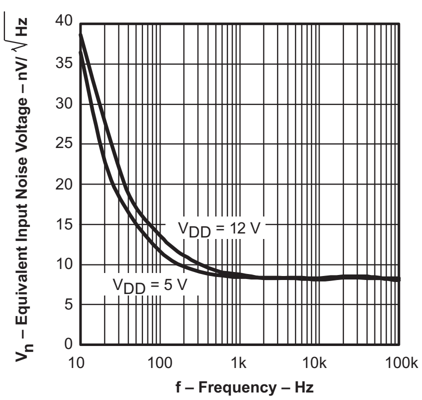


Figure 13.

PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

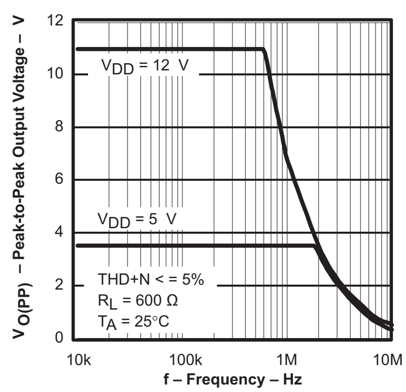


Figure 14.

PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

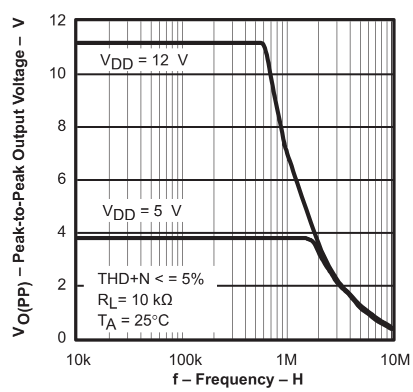


Figure 15.

CROSSTALK vs FREQUENCY

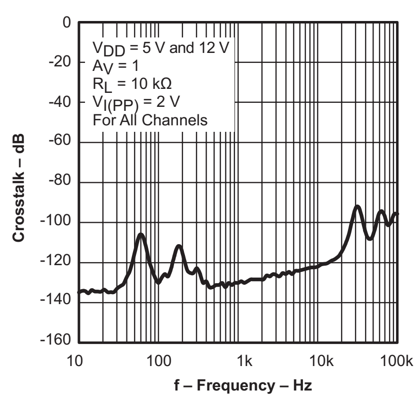


Figure 16.

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

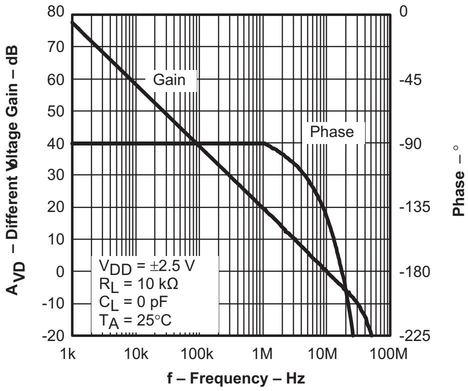


Figure 17.

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

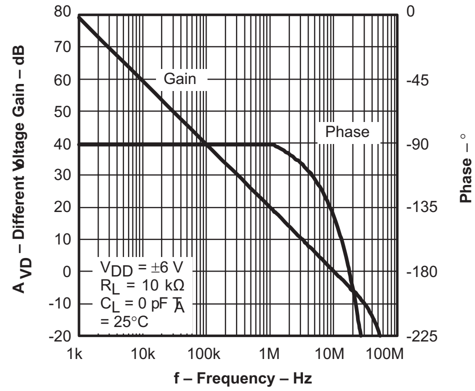


Figure 18.

PHASE MARGIN vs LOAD CAPACITANCE

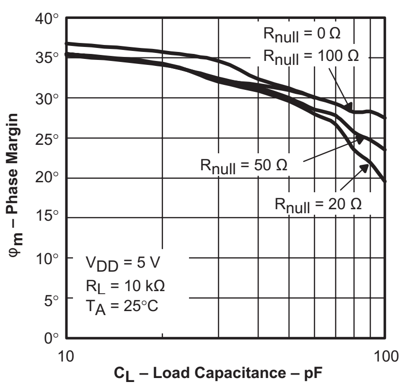


Figure 19.

PHASE MARGIN vs LOAD CAPACITANCE

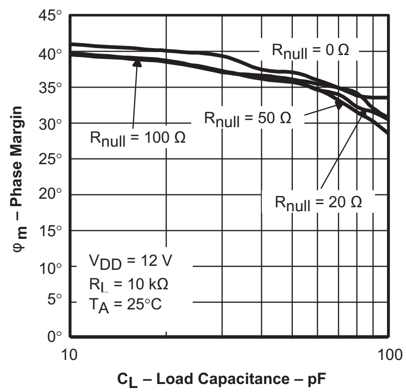


Figure 20.

GAIN MARGIN vs LOAD CAPACITANCE

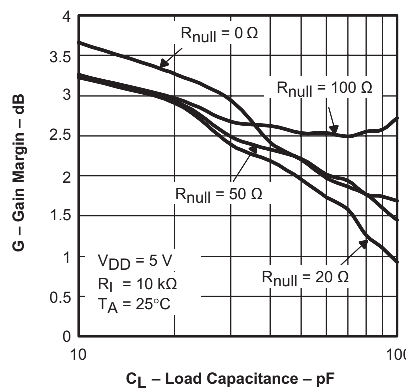


Figure 21.

GAIN MARGIN vs LOAD CAPACITANCE

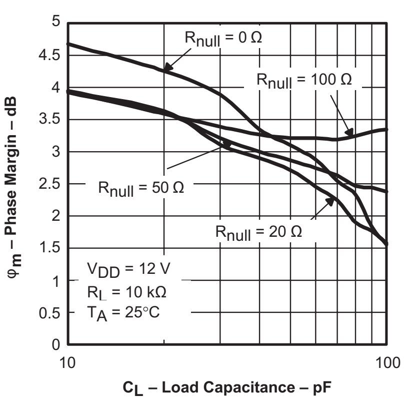


Figure 22.

GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

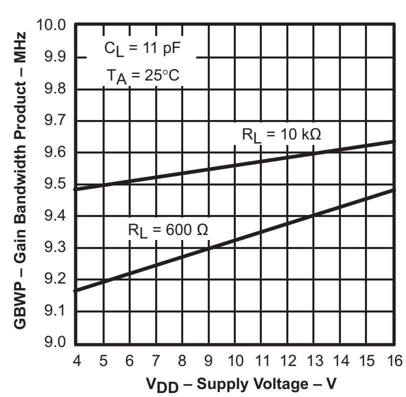


Figure 23.

SLEW RATE vs SUPPLY VOLTAGE

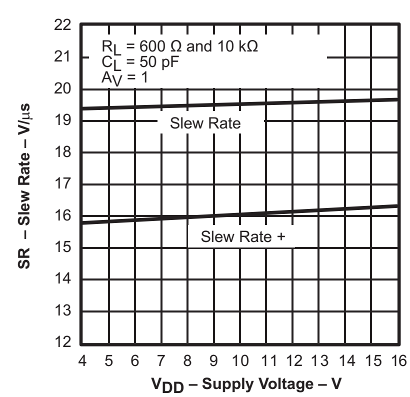


Figure 24.

TYPICAL CHARACTERISTICS

SLEW RATE vs FREE-AIR TEMPERATURE

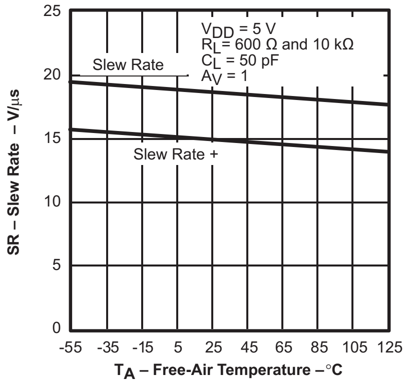


Figure 25.

SLEW RATE vs FREE-AIR TEMPERATURE

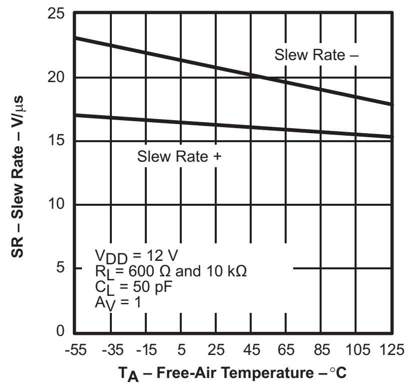


Figure 26.

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

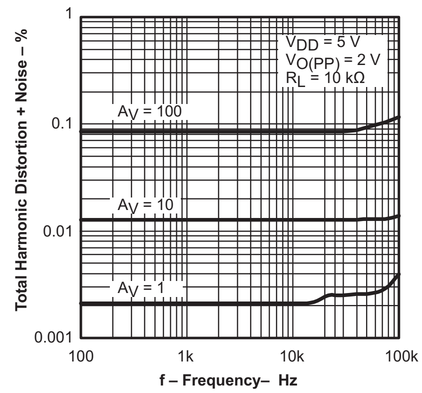


Figure 27.

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

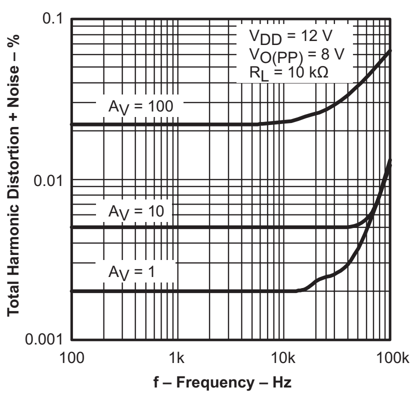


Figure 28.

TOTAL HARMONIC DISTORTION PLUS NOISE vs PEAK-TO-PEAK OUTPUT VOLTAGE

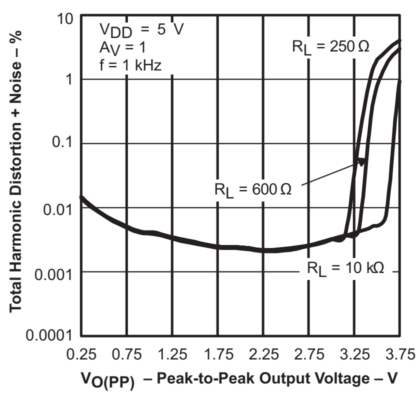


Figure 29.

TOTAL HARMONIC DISTORTION PLUS NOISE vs PEAK-TO-PEAK OUTPUT VOLTAGE

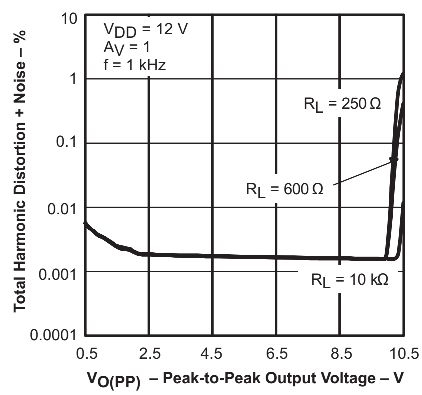


Figure 30.

LARGE SIGNAL FOLLOWER PULSE RESPONSE

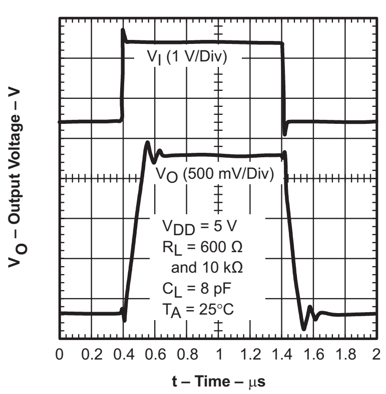


Figure 31.

LARGE SIGNAL FOLLOWER PULSE RESPONSE

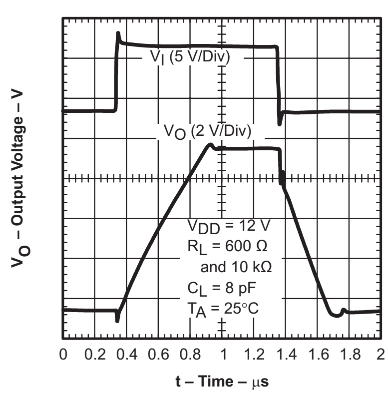


Figure 32.

SMALL SIGNAL FOLLOWER PULSE RESPONSE

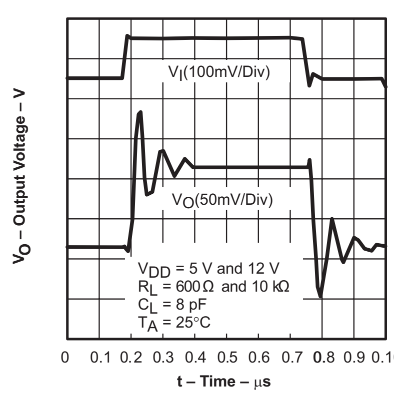


Figure 33.

TYPICAL CHARACTERISTICS

LARGE SIGNAL INVERTING PULSE RESPONSE

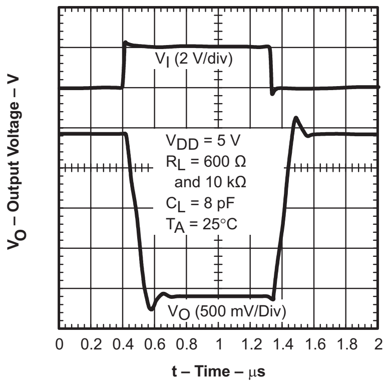


Figure 34.

LARGE SIGNAL INVERTING PULSE RESPONSE

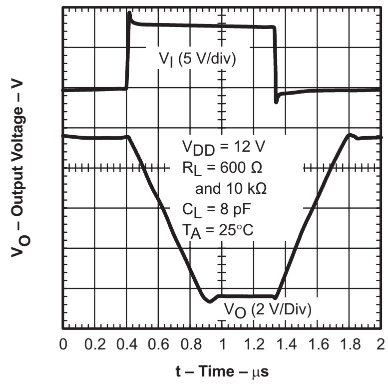


Figure 35.

SMALL SIGNAL INVERTING PULSE RESPONSE

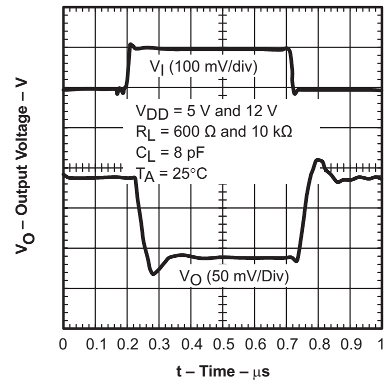


Figure 36.

SHUTDOWN FORWARD ISOLATION vs FREQUENCY

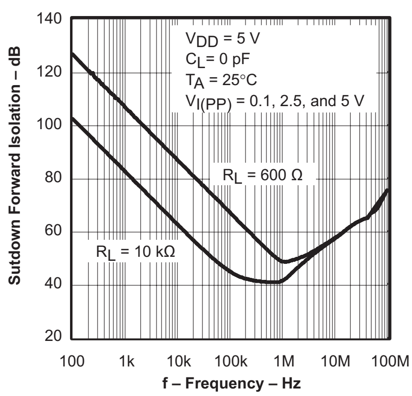


Figure 37.

SHUTDOWN FORWARD ISOLATION vs FREQUENCY

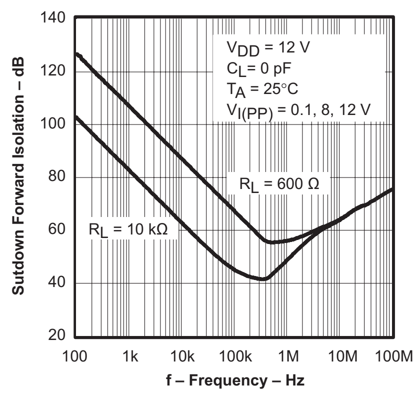


Figure 38.

SHUTDOWN REVERSE ISOLATION vs FREQUENCY

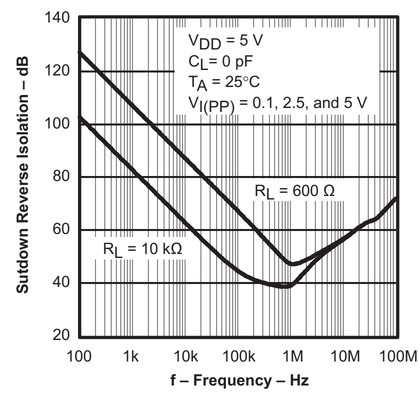


Figure 39.

SHUTDOWN REVERSE ISOLATION vs FREQUENCY

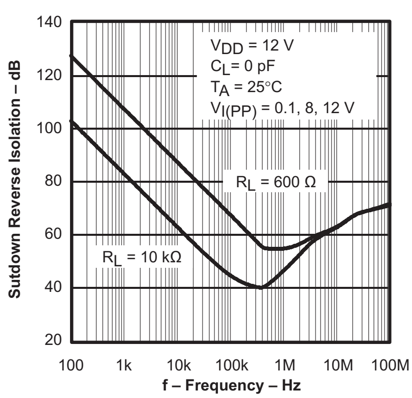


Figure 40.

SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE

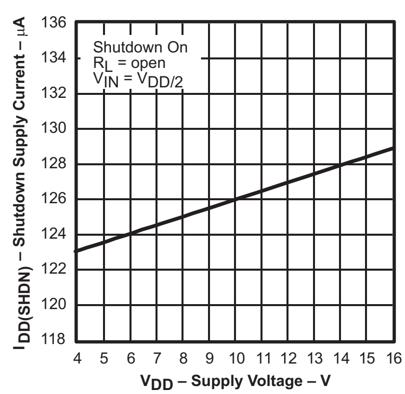


Figure 41.

SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE

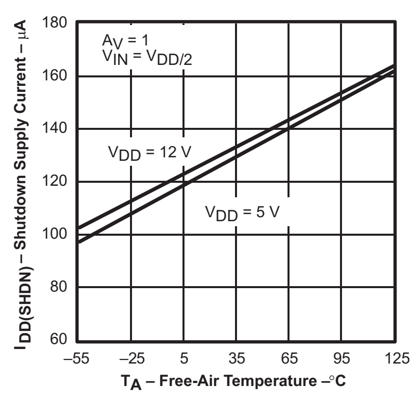


Figure 42.

TYPICAL CHARACTERISTICS

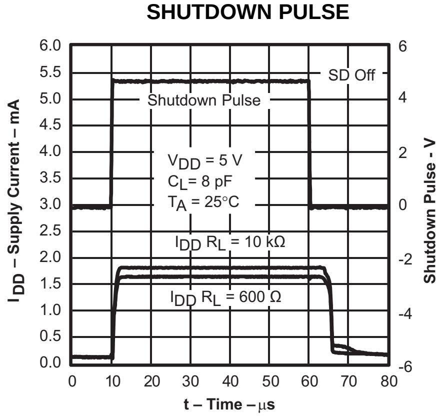


Figure 43.

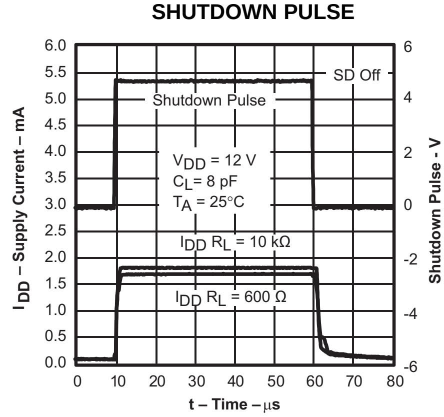


Figure 44.

PARAMETER MEASUREMENT INFORMATION

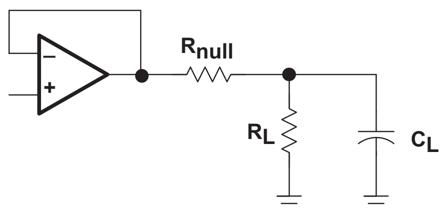


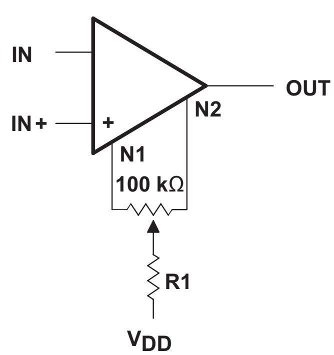
Figure 45

Figure 45.

APPLICATION INFORMATION

Input Offset Voltage Null Circuit

The TLC080 and TLC081 has an input offset nulling function. Refer to Figure 46 for the diagram.



A. R1 = 5.6 kΩ for offset voltage adjustment of ±10 mV. R1 = 20 kΩ for offset voltage adjustment of ±3 mV.

Figure 46. Input Offset Voltage Null Circuit

Driving a Capacitive Load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 47. A minimum value of 20 Ω should work well for most applications.

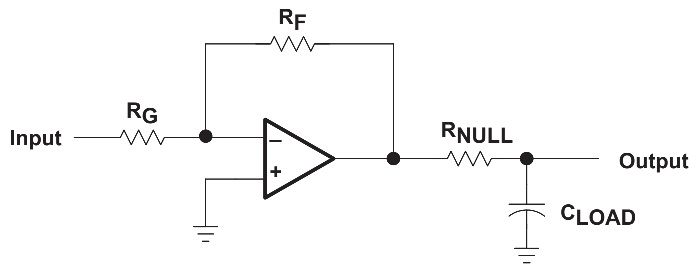
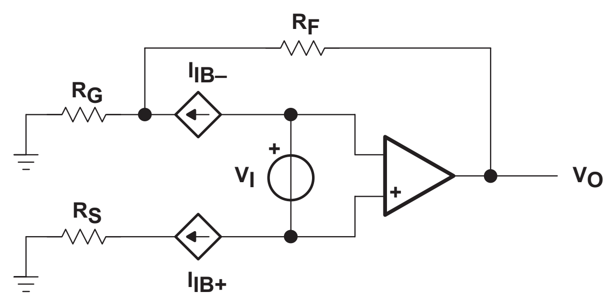


Figure 47. Driving a Capacitive Load

Offset Voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1+\left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}R_S\left(1+\left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}R_F$$

Figure 48. Output Offset Voltage Model

High Speed CMOS Input Amplifiers

The TLC08x is a family of high-speed low-noise CMOS input operational amplifiers that has an input capacitance of the order of 20 pF. Any resistor used in the feedback path adds a pole in the transfer function equivalent to the input capacitance multiplied by the combination of source resistance and feedback resistance. For example, a gain of –10, a source resistance of 1 kΩ, and a feedback resistance of 10 kΩ add an additional pole at approximately 8 MHz. This is more apparent with CMOS amplifiers than bipolar amplifiers due to their greater input capacitance.

This is of little consequence on slower CMOS amplifiers, as this pole normally occurs at frequencies above their unity-gain bandwidth. However, the TLC08x with its 10-MHz bandwidth means that this pole normally occurs at frequencies where there is on the order of 5dB gain left and the phase shift adds considerably.

The effect of this pole is the strongest with large feedback resistances at small closed loop gains. As the feedback resistance is increased, the gain peaking increases at a lower frequency and the 180° phase shift crossover point also moves down in frequency, decreasing the phase margin.

For the TLC08x, the maximum feedback resistor recommended is 5 kΩ; larger resistances can be used but a capacitor in parallel with the feedback resistor is recommended to counter the effects of the input capacitance pole.

The TLC083 with a 1-V step response has an 80% overshoot with a natural frequency of 3.5 MHz when configured as a unity gain buffer and with a 10-kΩ feedback resistor. By adding a 10-pF capacitor in parallel with the feedback resistor, the overshoot is reduced to 40% and eliminates the natural frequency, resulting in a much faster settling time (see Figure 49). The 10-pF capacitor was chosen for convenience only.

Load capacitance had little effect on these measurements due to the excellent output drive capability of the TLC08x.

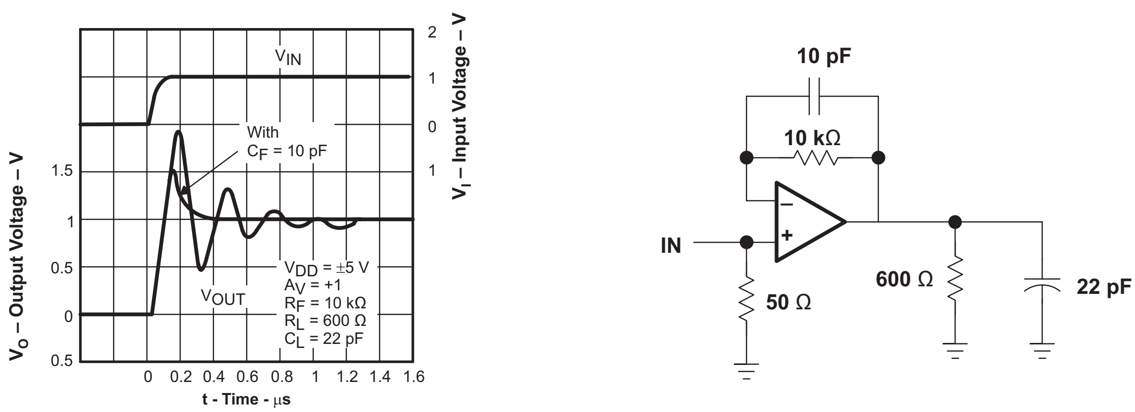
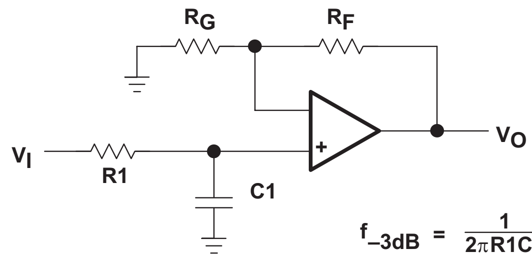


Figure 49. 1-V Step Response

General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into theFigure 50 system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see).

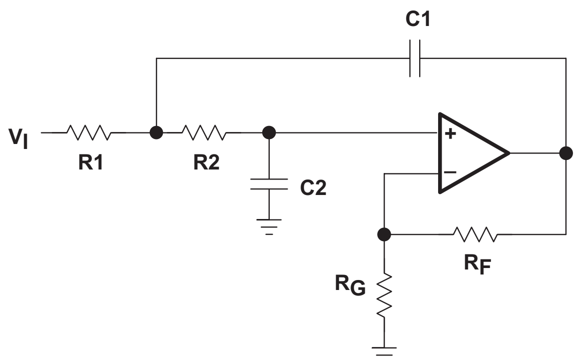


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 50. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 51. 2-Pole Low-Pass Sallen-Key Filter

Shutdown Function

Three members of the TLC08x family (TLC080/3/5) have a shutdown terminal (SHDN) for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 125 µA/channel, the amplifier is disabled, and the outputs are placed in a high-impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to the voltage on the GND terminal of the device. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to V_{DD-} (not system ground) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figure 43 and Figure 44. The amplifier is powered with a single 5-V supply and is configured as noninverting with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Figure 37 through Figure 40 show the amplifiers forward and reverse isolation in shutdown. The operational amplifier is configured as a voltage follower (A_V = 1). The isolation performance is plotted across frequency using 0.1 V_{PP}, 2.5 V_{PP}, and 5 V_{PP} input signals at ±2.5 V supplies and 0.1 V_{PP}, 8 V_{PP}, and 12 V_{PP} input signals at ±6 V supplies.

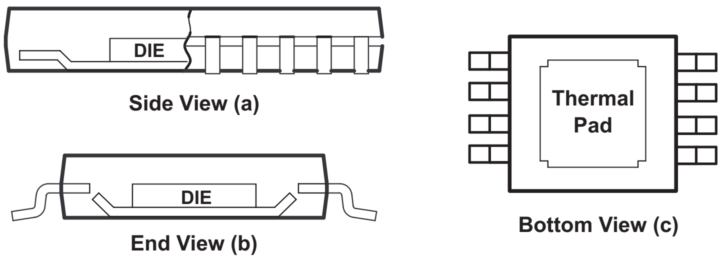
Circuit Layout Considerations

To achieve the levels of high performance of the TLC08x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

General PowerPAD Design Considerations

The TLC08x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 52(a) and Figure 52(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 52(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 52. Views of Thermally-Enhanced DGN Package

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. **Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation.** This soldering provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

The PowerPAD must be connected to the most negative supply voltage (GND pin potential) of the device.

1. Prepare the PCB with a top side etch pattern (see the landing patterns at the end of this data sheet). There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes (dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLC08x IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal plane that is at the same potential as the ground pin of the device.
5. When connecting these holes to this internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLC08x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the TLC08x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA}, the maximum power dissipation is shown in Figure 53 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right) \tag{1}$$

Where:

P_D = Maximum power dissipation of TLC08x IC (watts)

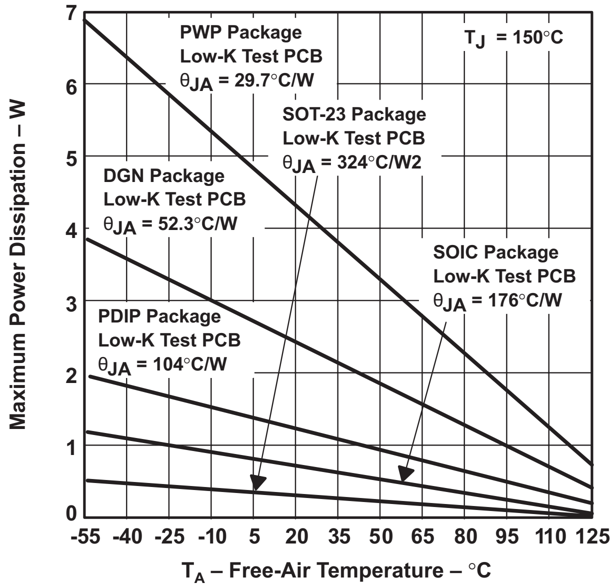
T_{MAX} = Absolute maximum junction temperature (150°C)

T_A = Free-ambient air temperature (°C)

θ_{JA} = $\theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case

θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



A. Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 53. Maximum Power Dissipation vs Free-Air Temperature

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents.

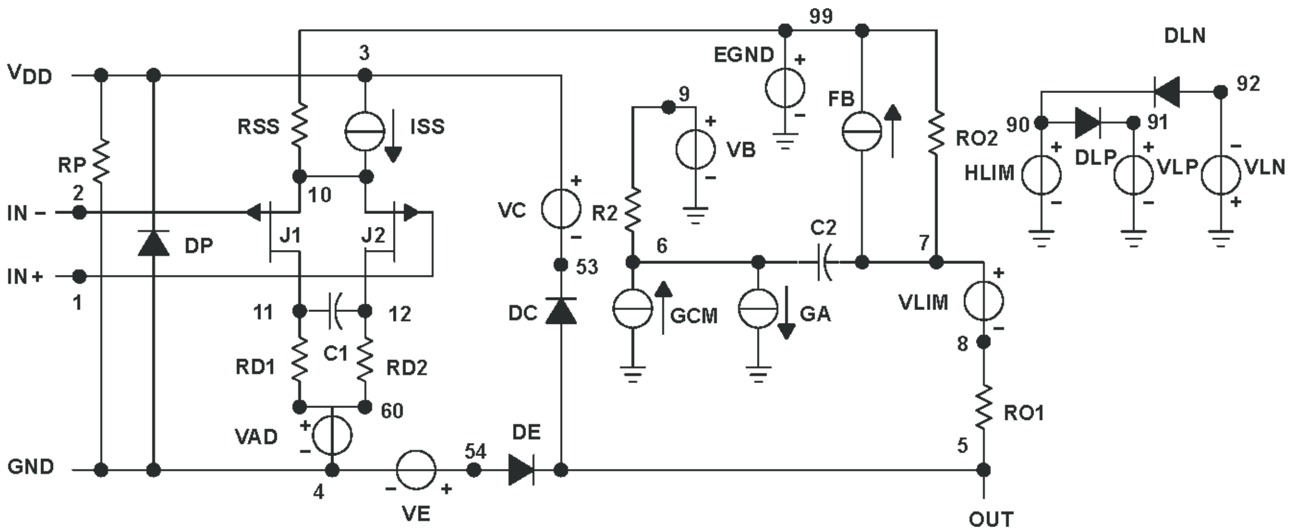
The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

Macromodel Information

Macromodel information provided was derived using Microsim Parts™, the model generation software used with Microsim PSpice™. The Boyle macromodel (see [(1)]) and subcircuit in Figure 54 are generated using the TLC08x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,” IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).




```
*DEVICE=TLC08X_5V, OPAMP, PJF, INT

* TLC08X_5V − 5V operational amplifier "macromodel" sub-
circuit
* created using Parts release 8.0 on 12/16/99 at 14:03
* Parts is a MicroSim product.
*
* connections:     non-inverting input
*                  | inverting input
*                  | | positive power supply
*                  | | | negative power supply
*                  | | | | output
*                  | | | | |
.subckt TLC08X_5V  1 2 3 4 5
*
 c1    11  12  4.6015E−12
 c2    6   7   8.0000E−12
 css   10  99  986.29E−15
 dc    5   53  dy
 de    54  5   dy
 dlp   90  91  dx
 dln   92  90  dx
 dp    4   3   dx
 egnd  99  0   poly(2) (3,0) (4,0) 0 .5 .5
 fb    7   99  poly(5) vb vc ve vlp vln 0 13.984E6 −1E3 1E3
               14E6 −14E6
 ga    6   0   11   12 402.12E−6
 gcm   0   6   10   99 1.5735E−6
 ioff  0   6   dc   1.212E−6
 iss   3   10  dc   130.40E−6
 hlim  90  0   vlim 1K
 j1    11  2   10   jx1
 j2    12  1   10   jx2
 r2    6   9        100.00E3
 rd1   4   11       2.4868E3
 rd2   4   12       2.4868E3
 ro1   8   5   10
 ro2   7   99  10
 rp    3   4        2.8249E3
 rss   10  99       1.5337E6
 vb    9   0   dc   0
 vc    3   53  dc   1.5537
 ve    54  4   dc   .84373
 vlim  7   8   dc   0
 vlp   91  0   dc   117.60
 vln   0   92  dc   117.60
.model dx  D(Is=800.00E−18)
.model dy  D(Is=800.00E−18 Rs=1m Cjo=10p)
.model jx1 PJF(Is=80.000E−15 Beta=1.2401E−3  Vto=−1)
.model jx2 PJF(Is=80.000E−15 Beta=1.2401E−3  Vto=−1)
.ends
```

Figure 54. Boyle Macromodel and Subcircuit

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2006) to Revision F	Page
• Updated Figure 9	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC080AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C080AI	Samples
TLC080AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	TLC080AI	Samples
TLC080CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	C080C	Samples
TLC080CDGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACW	Samples
TLC080CDGNRG4	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACW	Samples
TLC080CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	C080C	Samples
TLC080ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C080I	Samples
TLC080IDGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ACX	Samples
TLC080IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C080I	Samples
TLC080IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	TLC080I	Samples
TLC081AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C081AI	Samples
TLC081AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C081AI	Samples
TLC081AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	TLC081AI	Samples
TLC081CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	C081C	Samples
TLC081CDGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACY	Samples
TLC081CDGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACY	Samples
TLC081CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	C081C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC081CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TLC081C	Samples
TLC081ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C081I	Samples
TLC081IDGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ACZ	Samples
TLC081IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C081I	Samples
TLC081IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C081I	Samples
TLC081IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	TLC081I	Samples
TLC082AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C082AI	Samples
TLC082AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C082AI	Samples
TLC082AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C082AI	Samples
TLC082AIP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	C082AI	Samples
TLC082CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	C082C	Samples
TLC082CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	C082C	Samples
TLC082CDGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ADZ	Samples
TLC082CDGNG4	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ADZ	Samples
TLC082CDGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	ADZ	Samples
TLC082CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	C082C	Samples
TLC082CP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	C082C	Samples
TLC082ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C082I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC082IDGN	ACTIVE	HVSSOP	DGN	8	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AEA	Samples
TLC082IDGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AEA	Samples
TLC082IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C082I	Samples
TLC082IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C082I	Samples
TLC082IP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	C082I	Samples
TLC083AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C083AI	Samples
TLC083CDGQR	ACTIVE	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	AEB	Samples
TLC083CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	C083C	Samples
TLC083CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	C083C	Samples
TLC083IDGQ	ACTIVE	HVSSOP	DGQ	10	80	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AEC	Samples
TLC083IN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	C083I	Samples
TLC084AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC084AI	Samples
TLC084AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC084AI	Samples
TLC084AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC084AI	Samples
TLC084AIN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	TLC084AI	Samples
TLC084AIPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC084AI	Samples
TLC084AIPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC084AI	Samples
TLC084CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC084C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC084CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC084C	Samples
TLC084CN	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TLC084C	Samples
TLC084CNE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TLC084C	Samples
TLC084CPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLC084C	Samples
TLC084CPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLC084C	Samples
TLC084ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC084I	Samples
TLC084IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC084I	Samples
TLC084IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC084I	Samples
TLC084IPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC084I	Samples
TLC084IPWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC084I	Samples
TLC085AID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC085AI	Samples
TLC085AIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC085AI	Samples
TLC085AIN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	TLC085AI	Samples
TLC085AIPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC085AI	Samples
TLC085CN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	TLC085C	Samples
TLC085CPWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLC085C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC082, TLC084 :

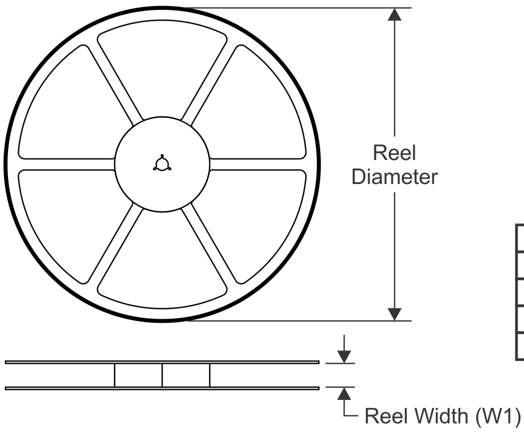
- Automotive: TLC082-Q1, TLC084-Q1

NOTE: Qualified Version Definitions:

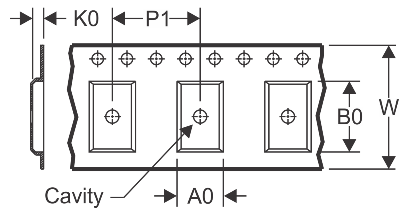
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

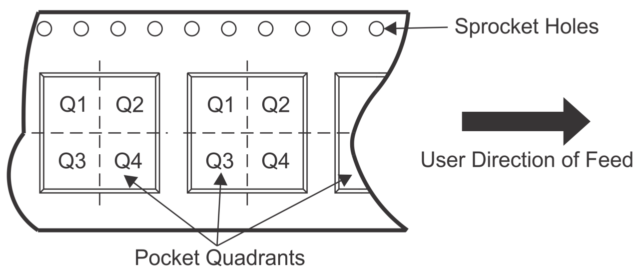


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

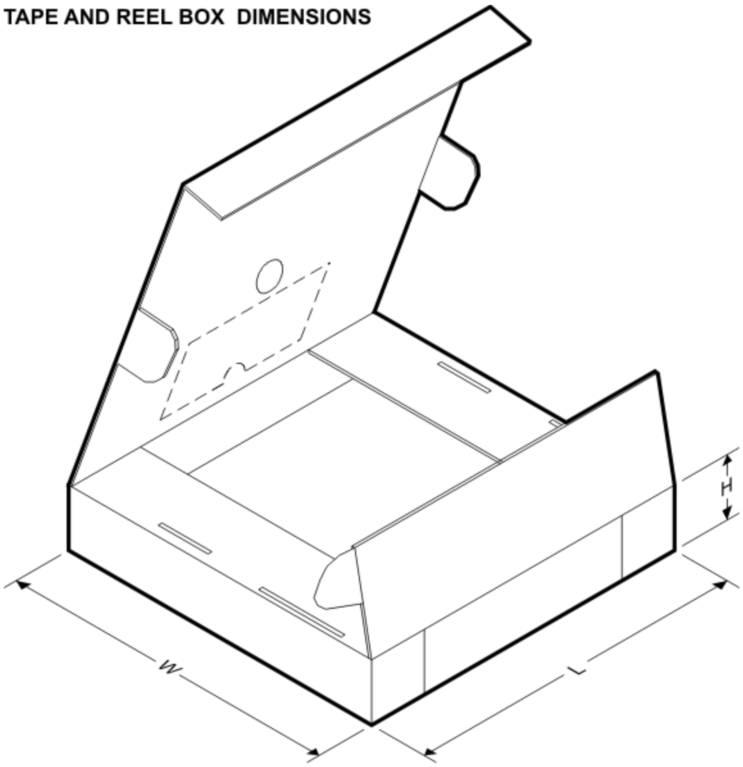


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC080AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC080CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLC080CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC080IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLC080IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC081AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC081CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLC081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC081IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLC081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC082AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC082CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLC082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC082IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLC082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC083CDGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLC083CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC084AIPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC084CPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC084IPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC085AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

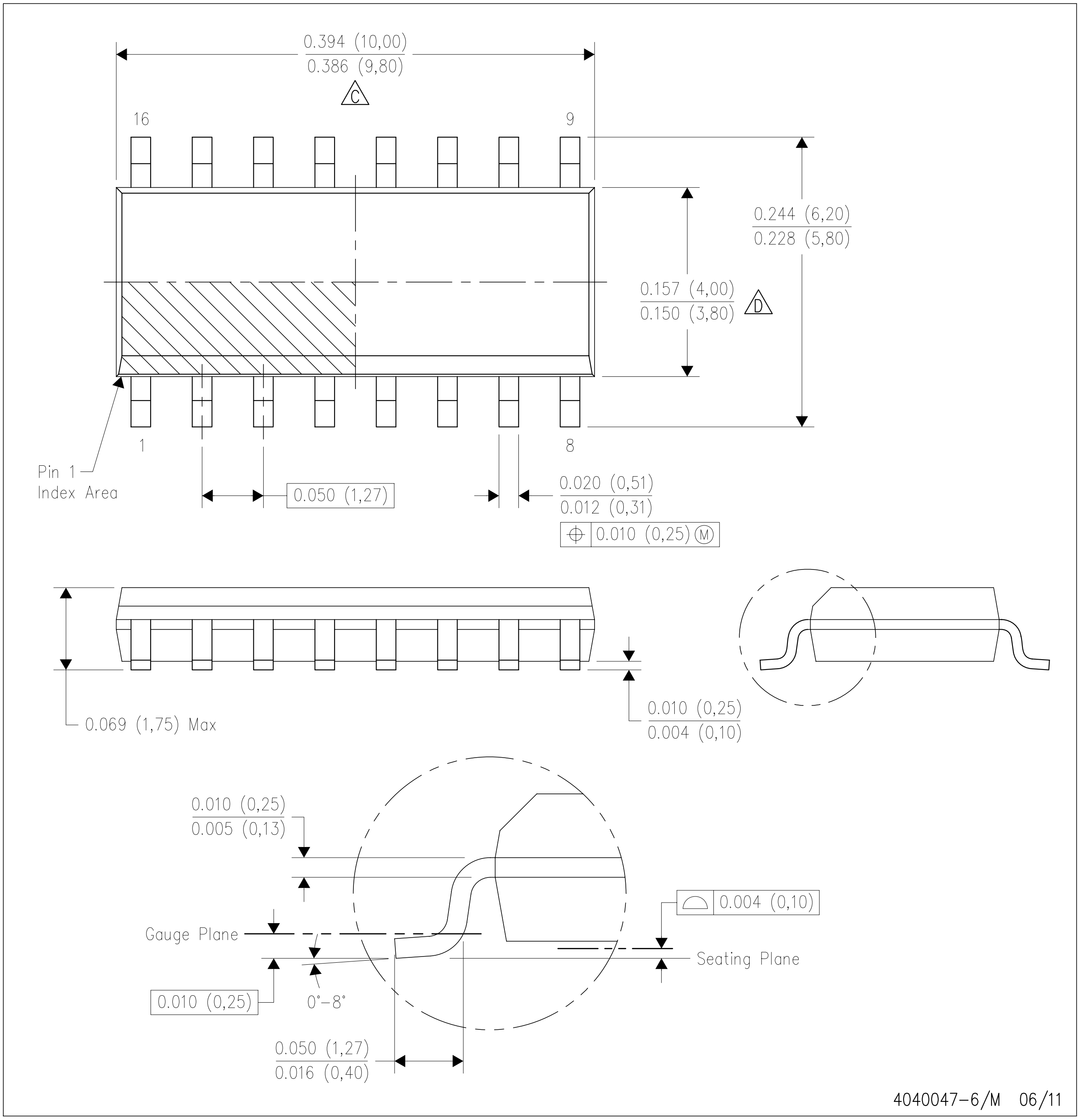


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC080AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC080CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TLC080CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC080IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TLC080IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC081AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC081CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TLC081CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC081IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TLC081IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC082AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC082CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TLC082CDR	SOIC	D	8	2500	340.5	338.1	20.6

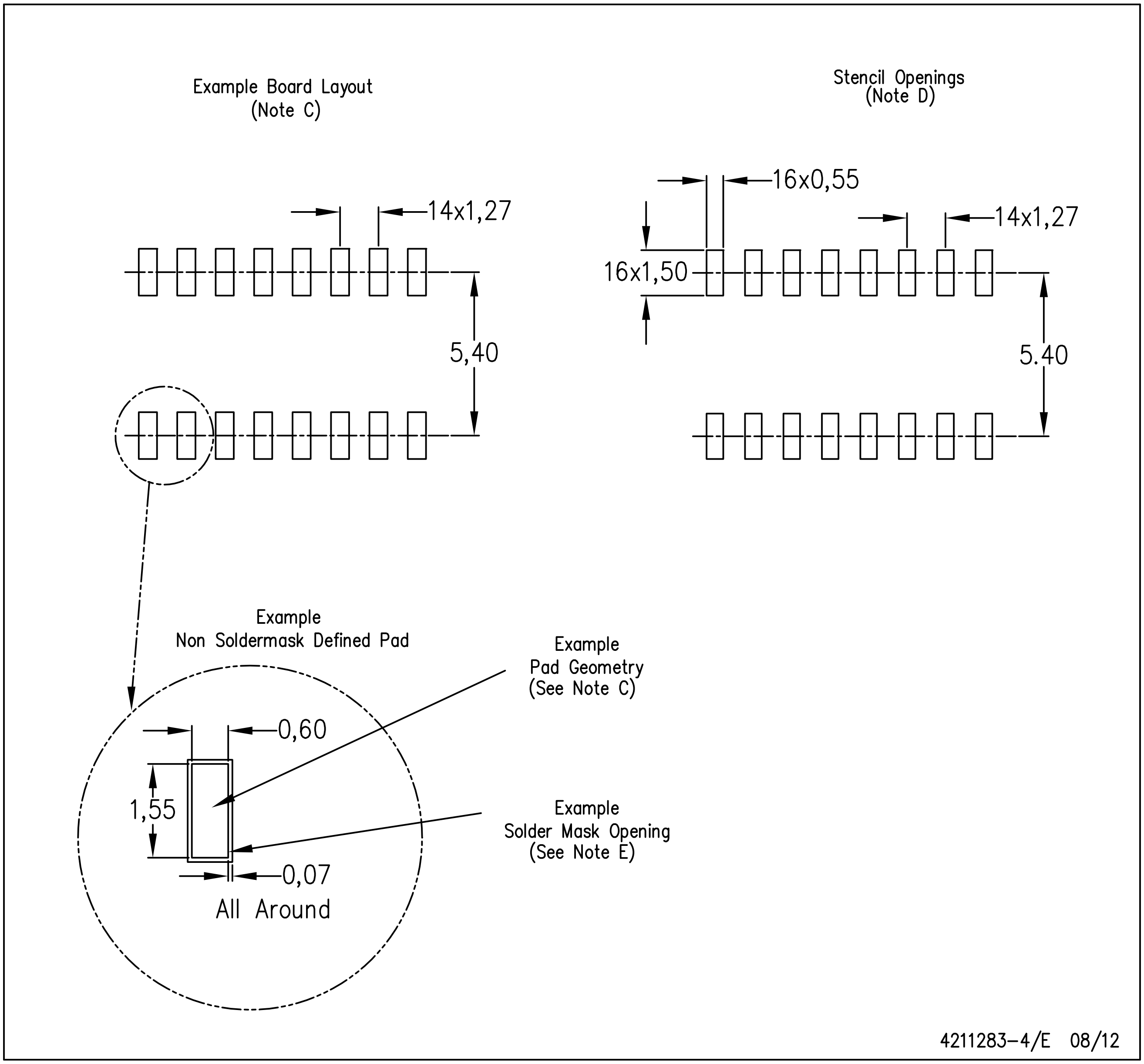
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC082IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TLC082IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC083CDGQR	HVSSOP	DGQ	10	2500	358.0	335.0	35.0
TLC083CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC084AIPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TLC084CPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TLC084IDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC084IPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TLC085AIDR	SOIC	D	16	2500	350.0	350.0	43.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



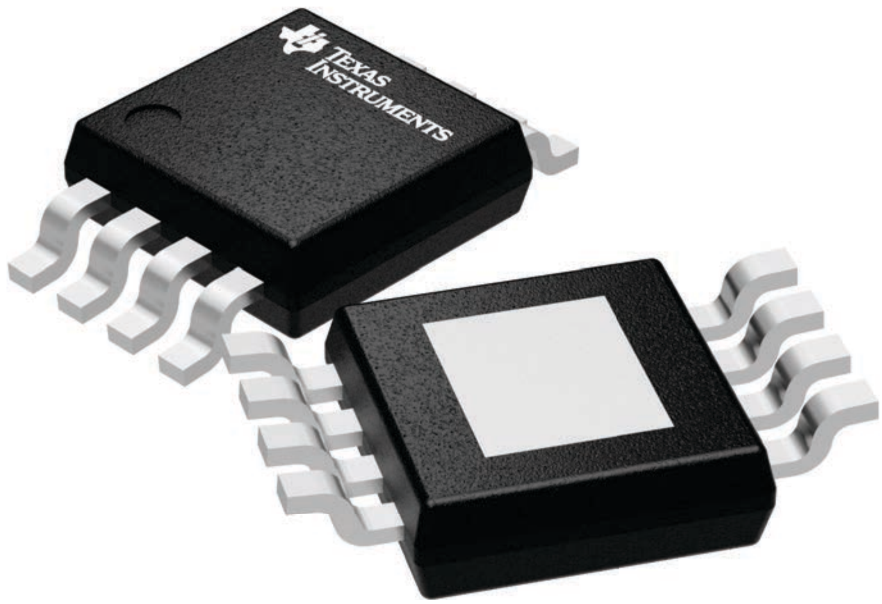
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

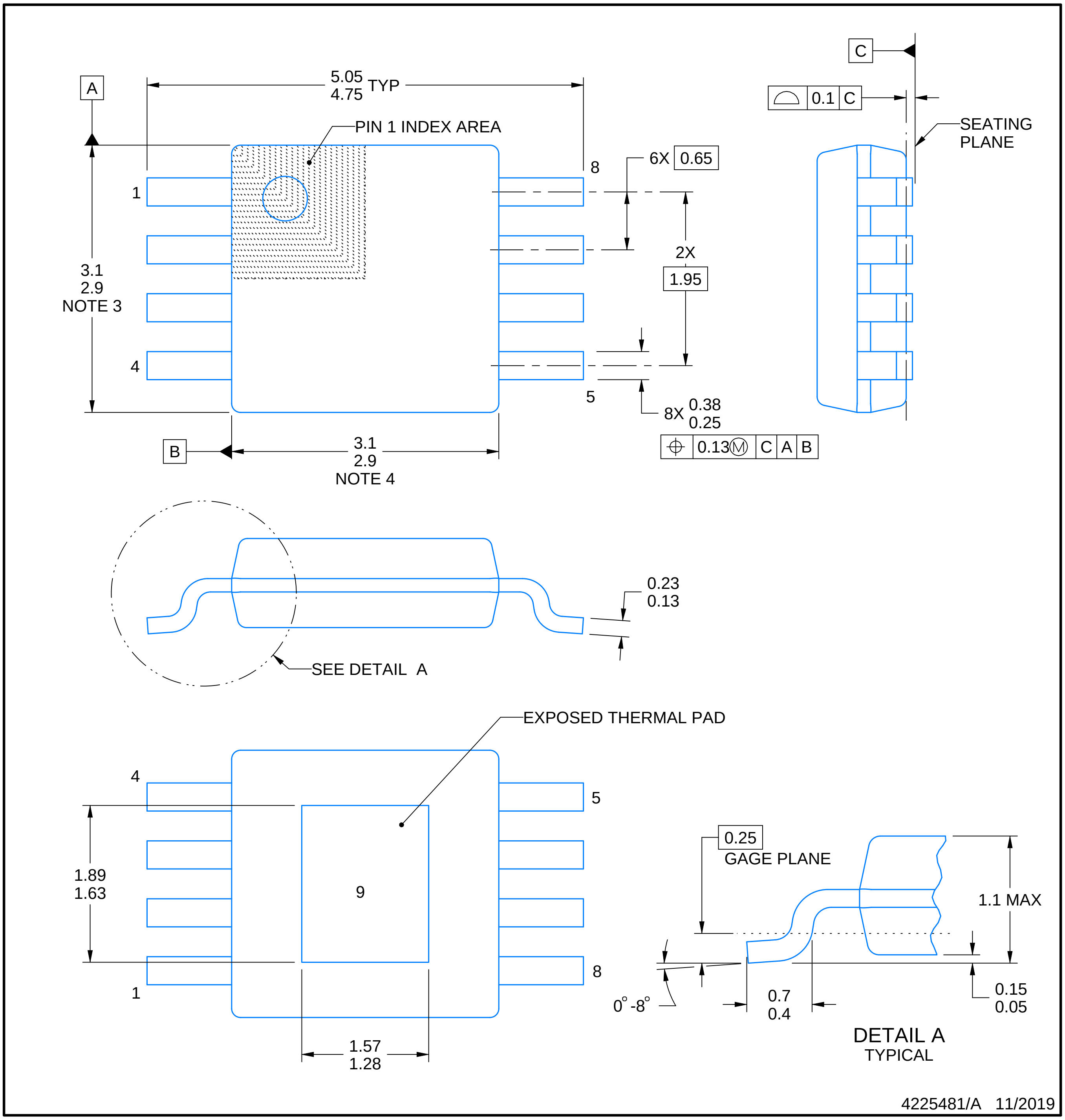


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



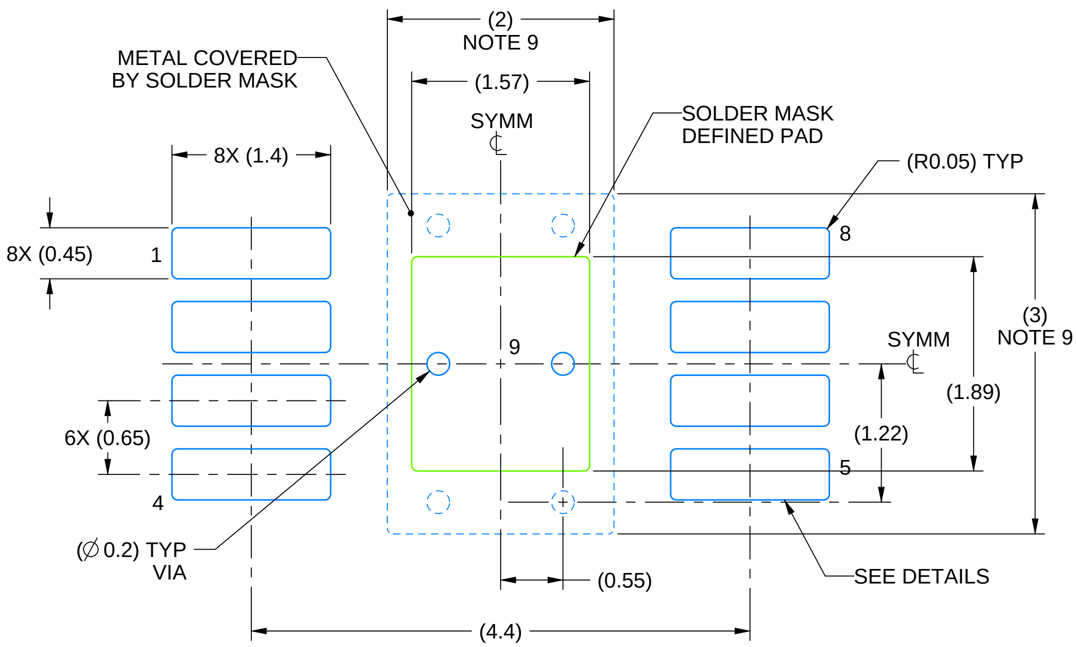
4225482/A



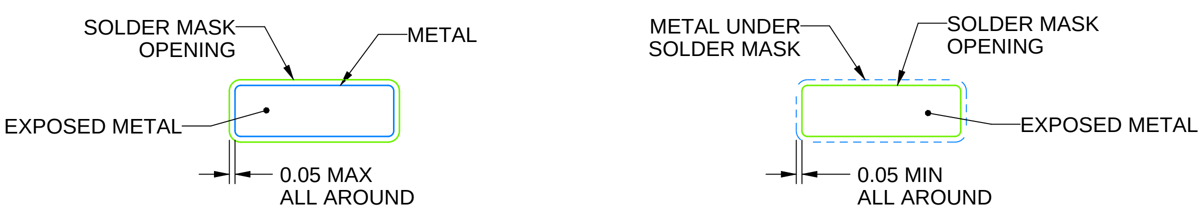
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

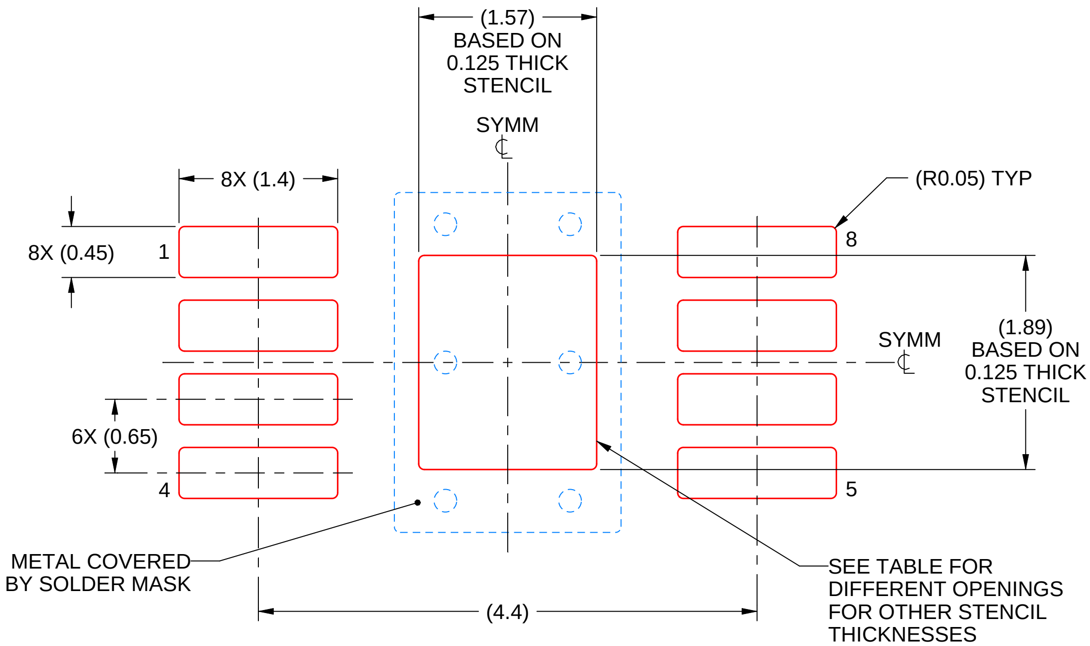
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

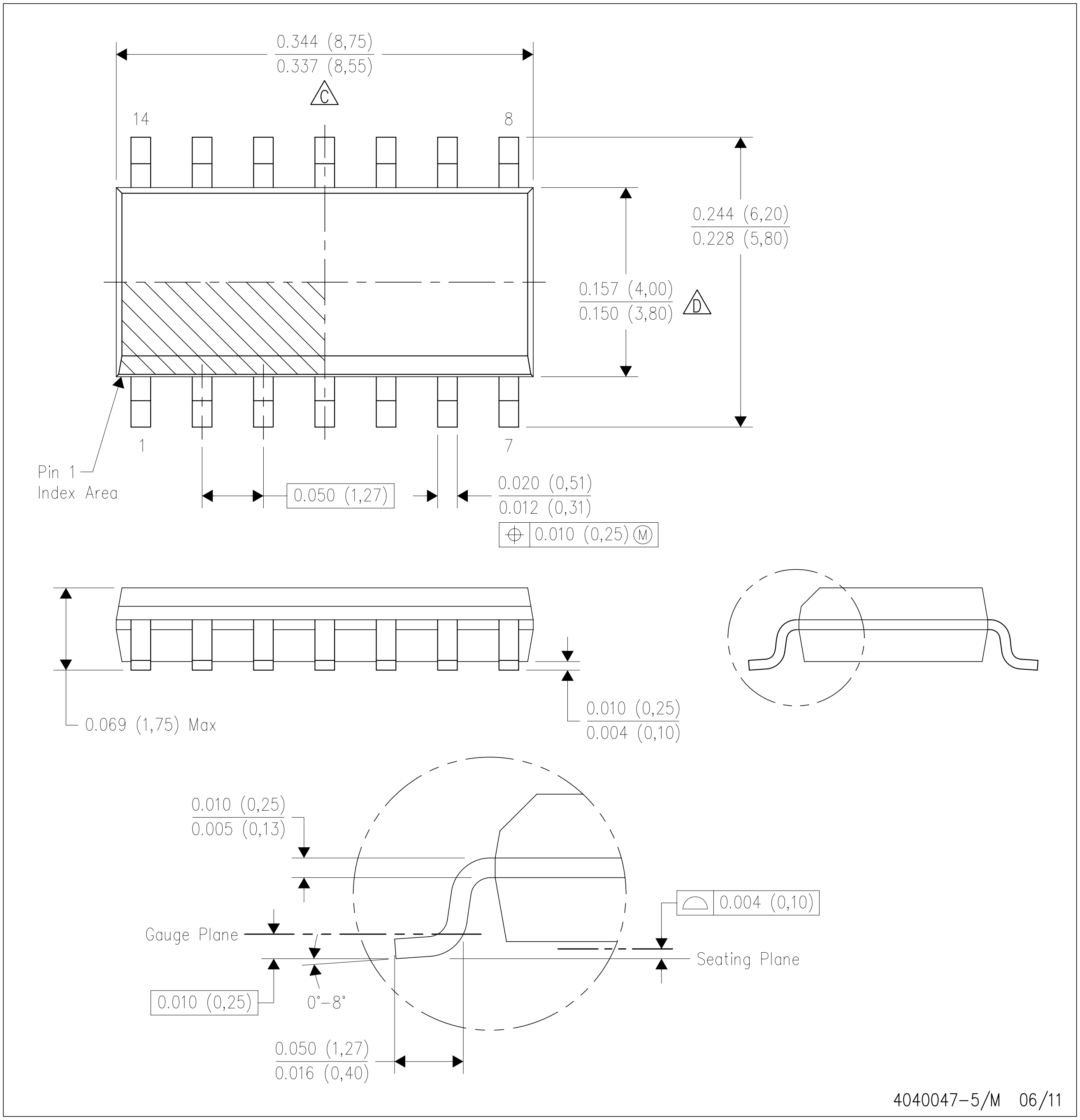
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

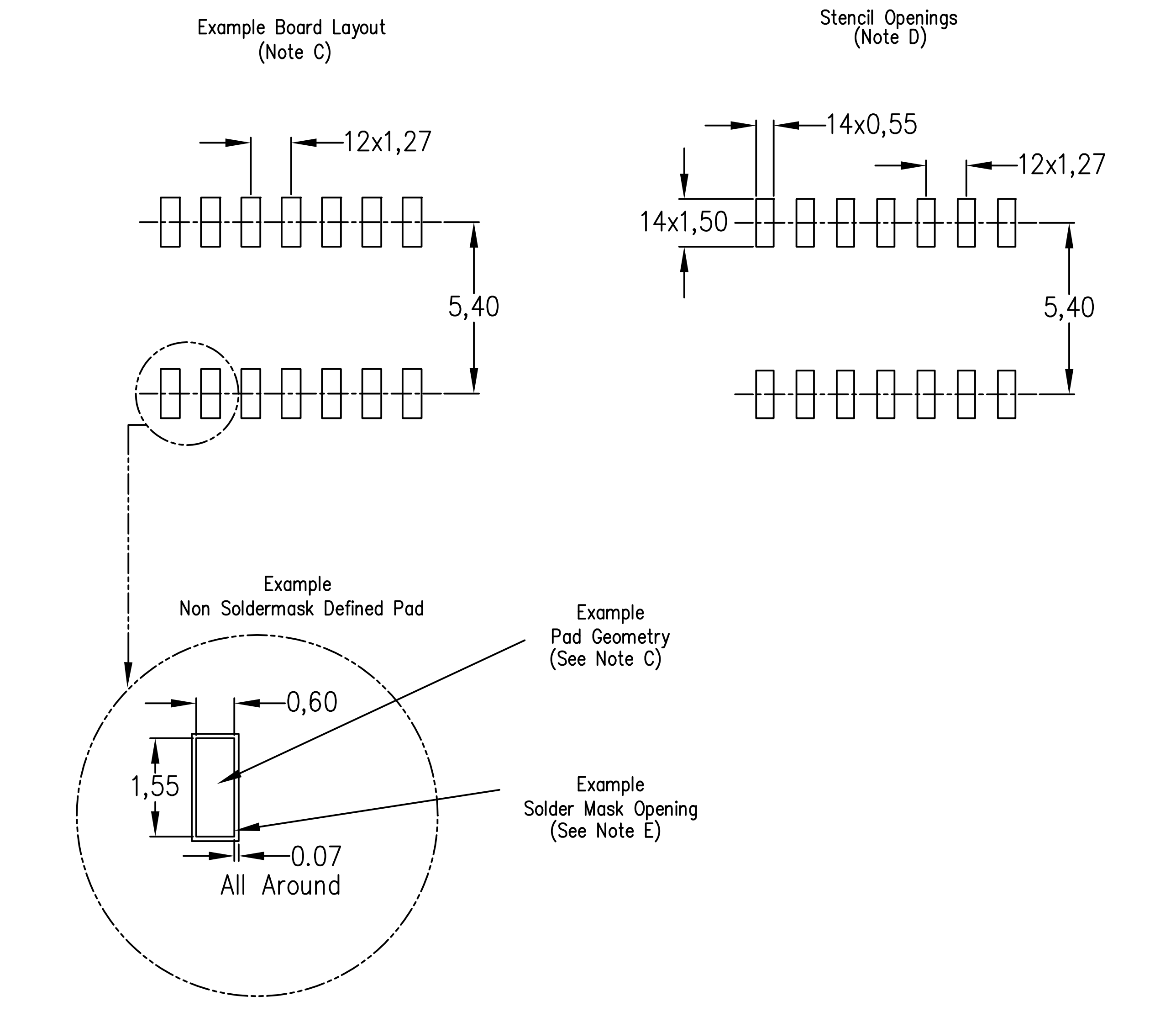
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



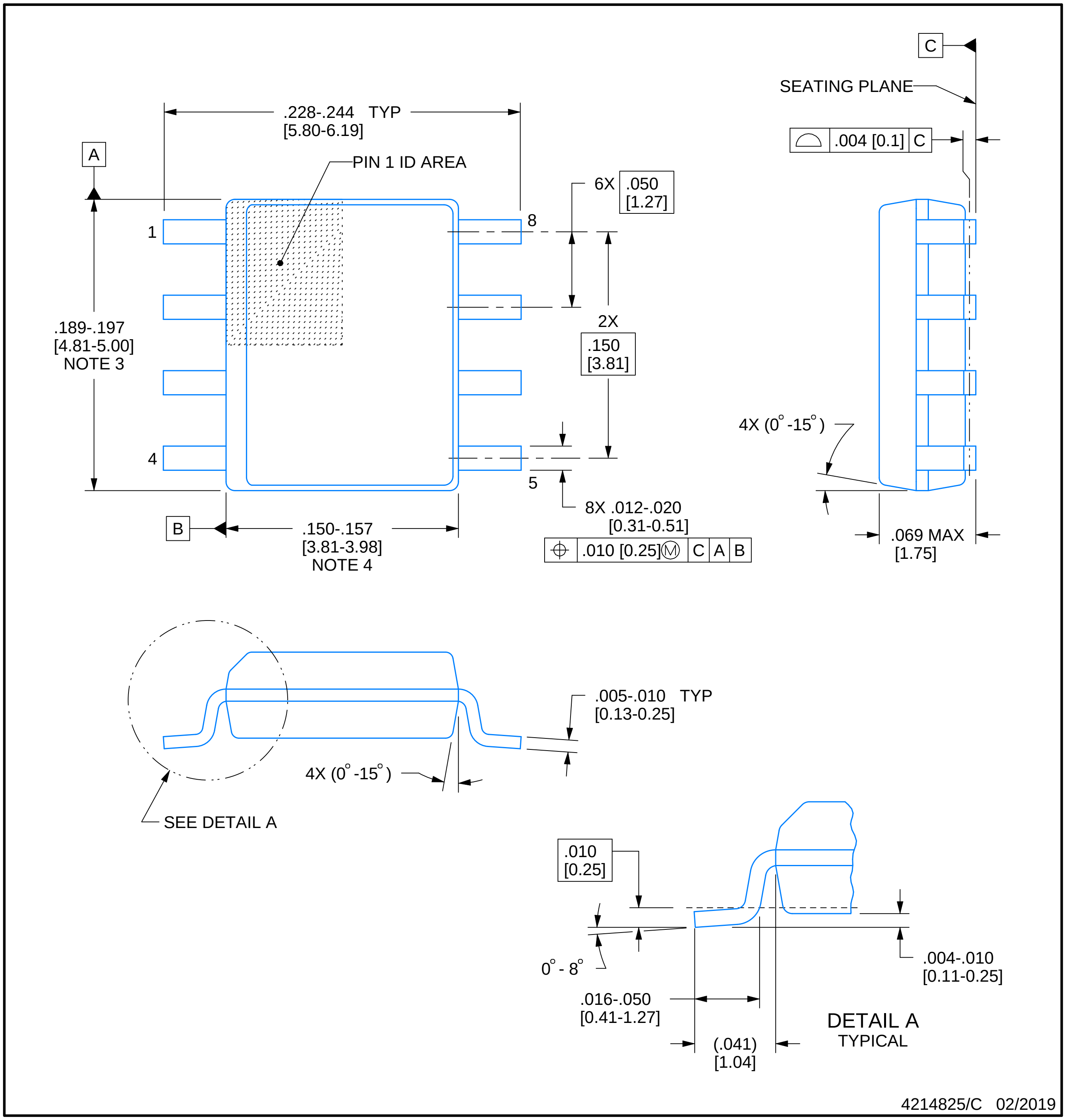
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211283-3/E 08/12

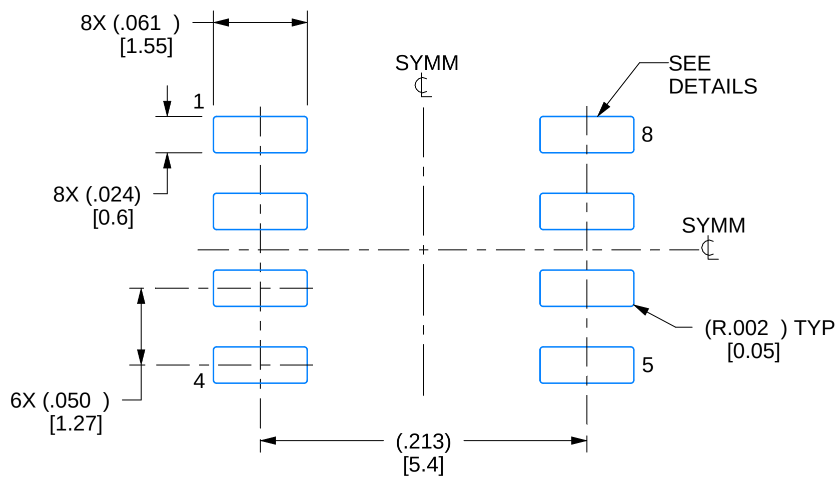
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



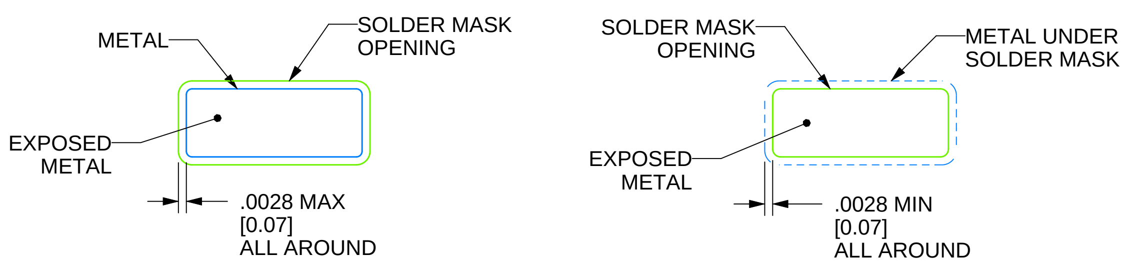
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

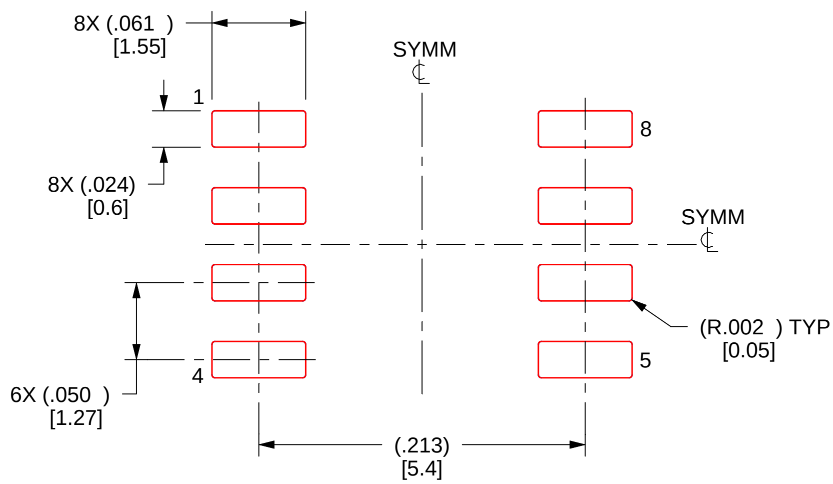
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



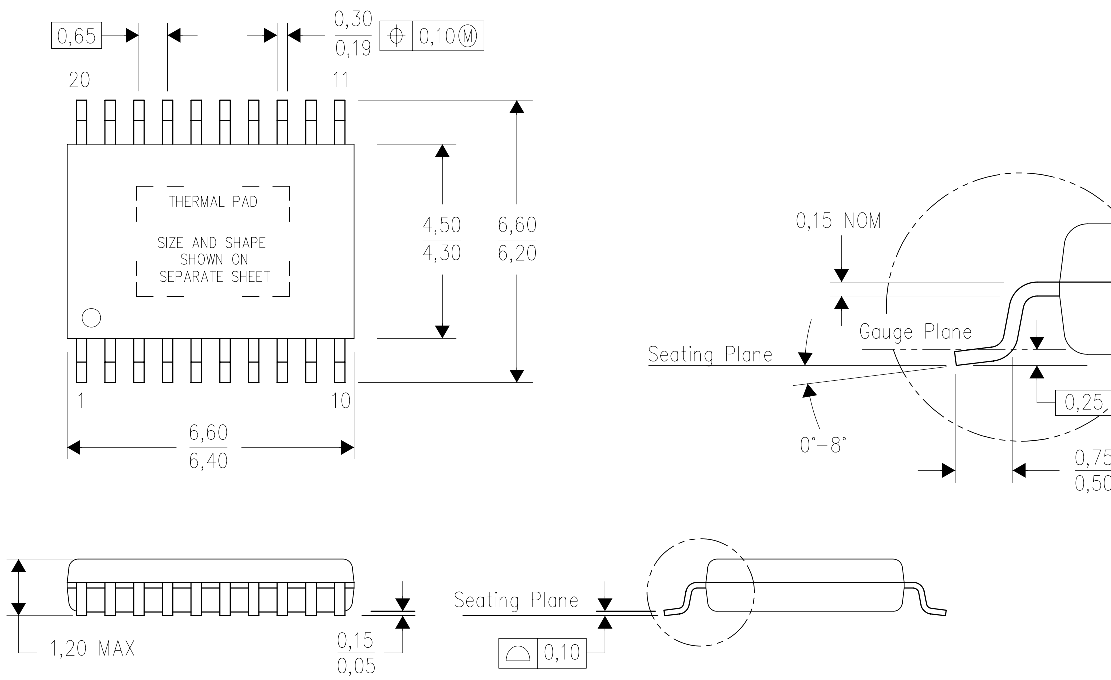
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

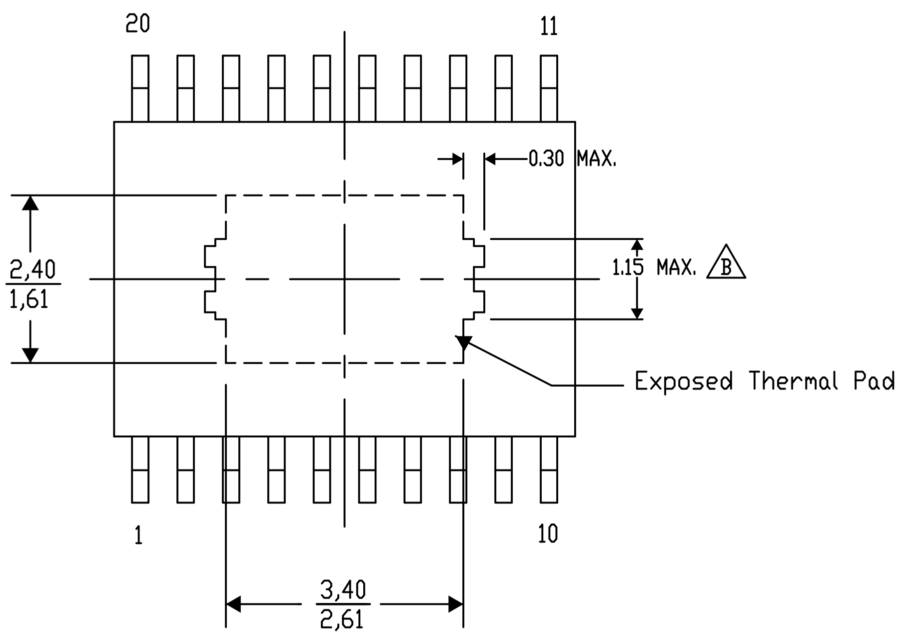
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

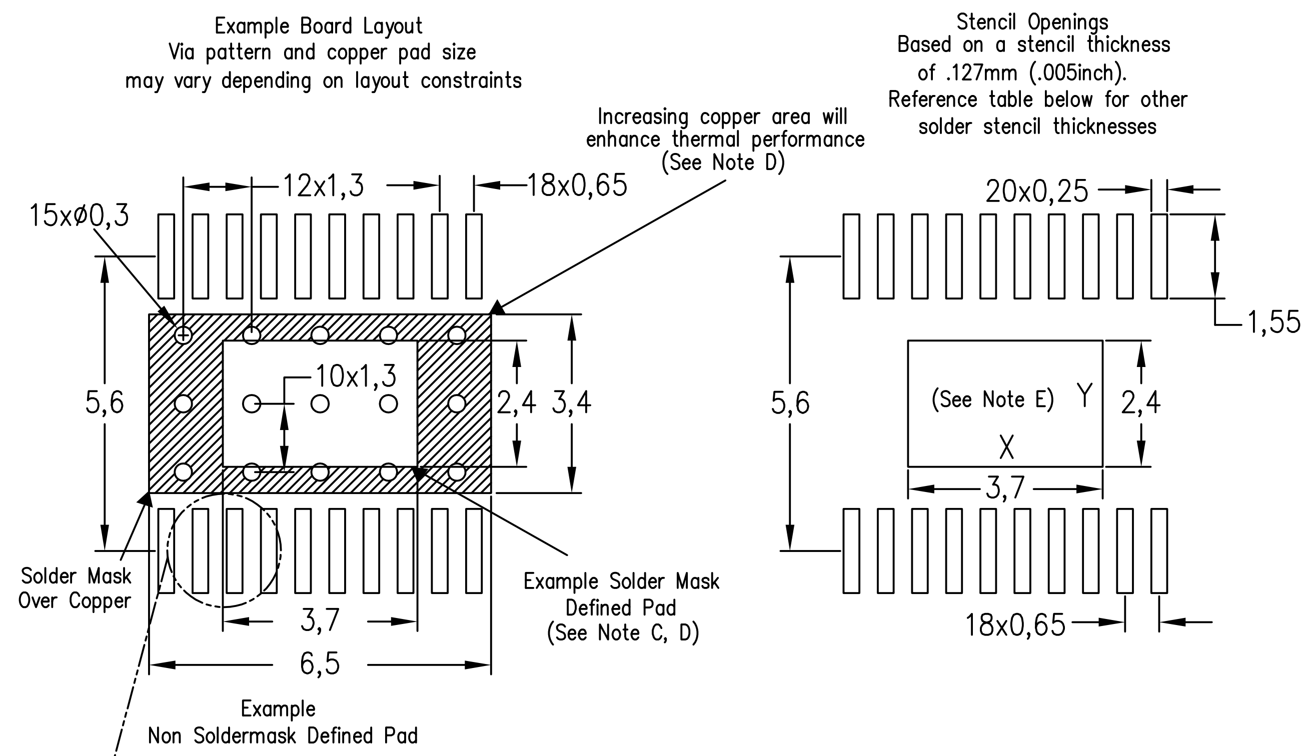
4206332-15/A0 01/16

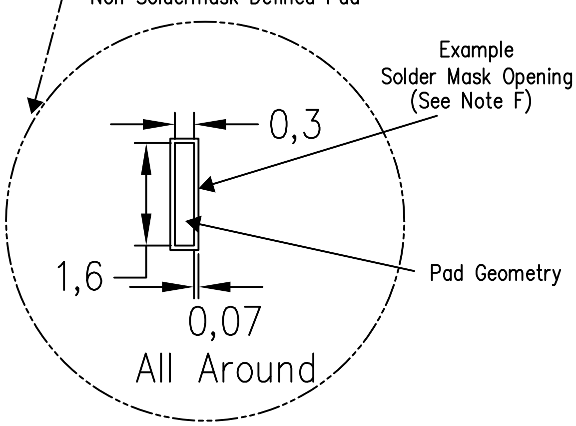
NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE



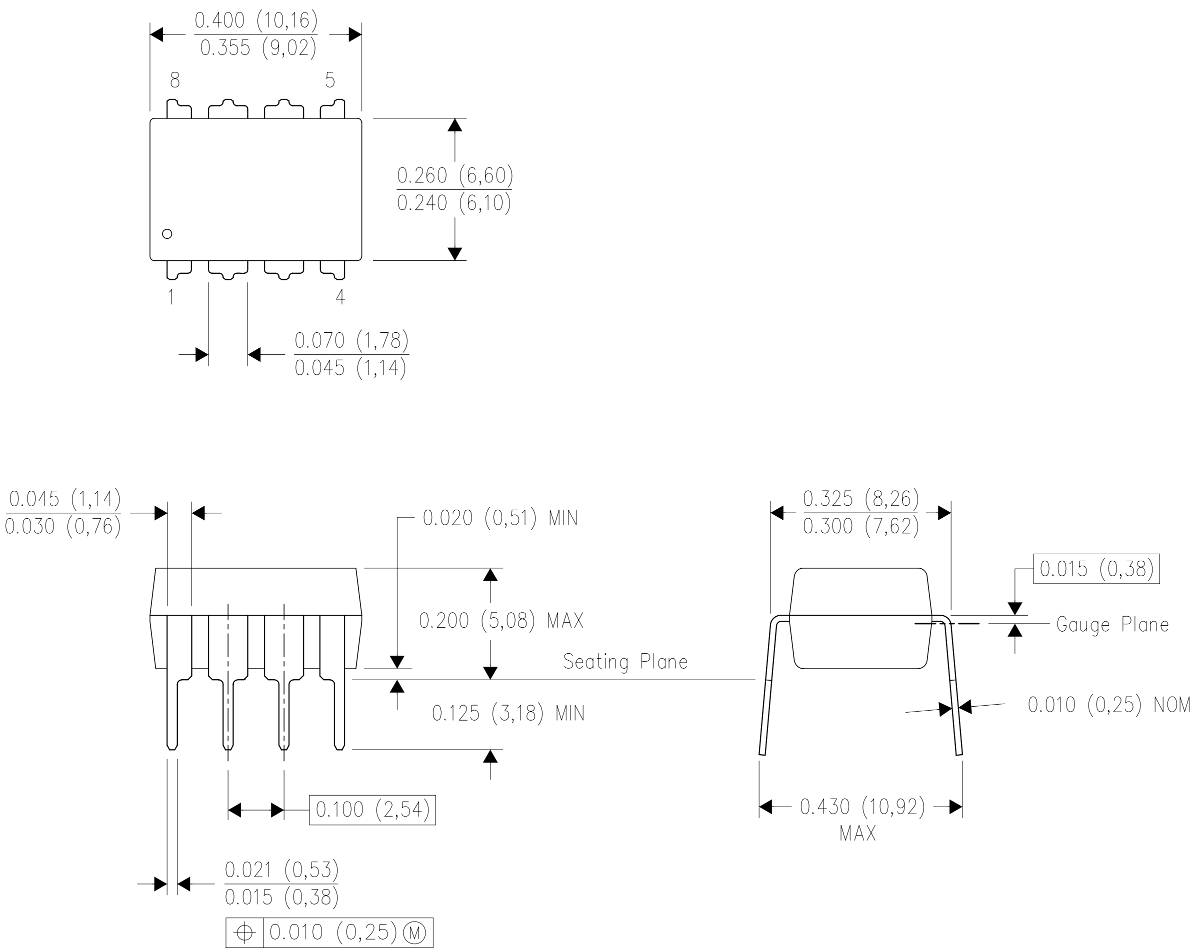


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609-8/W 09/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

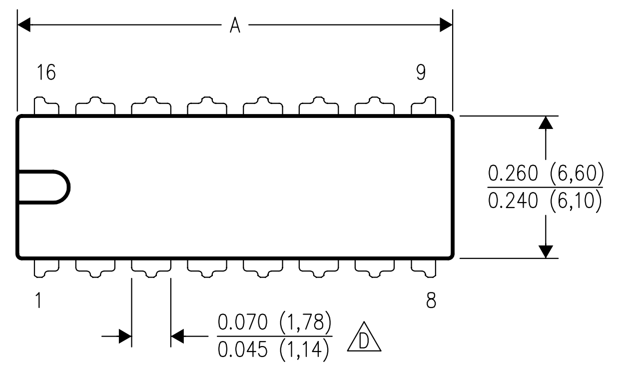


4040082/E 04/2010

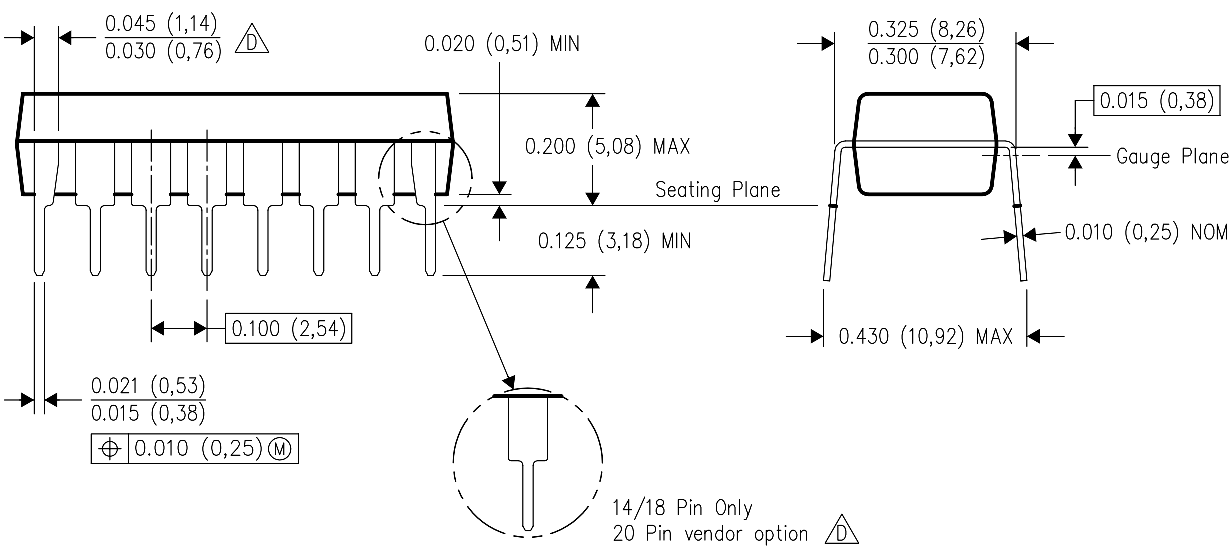
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



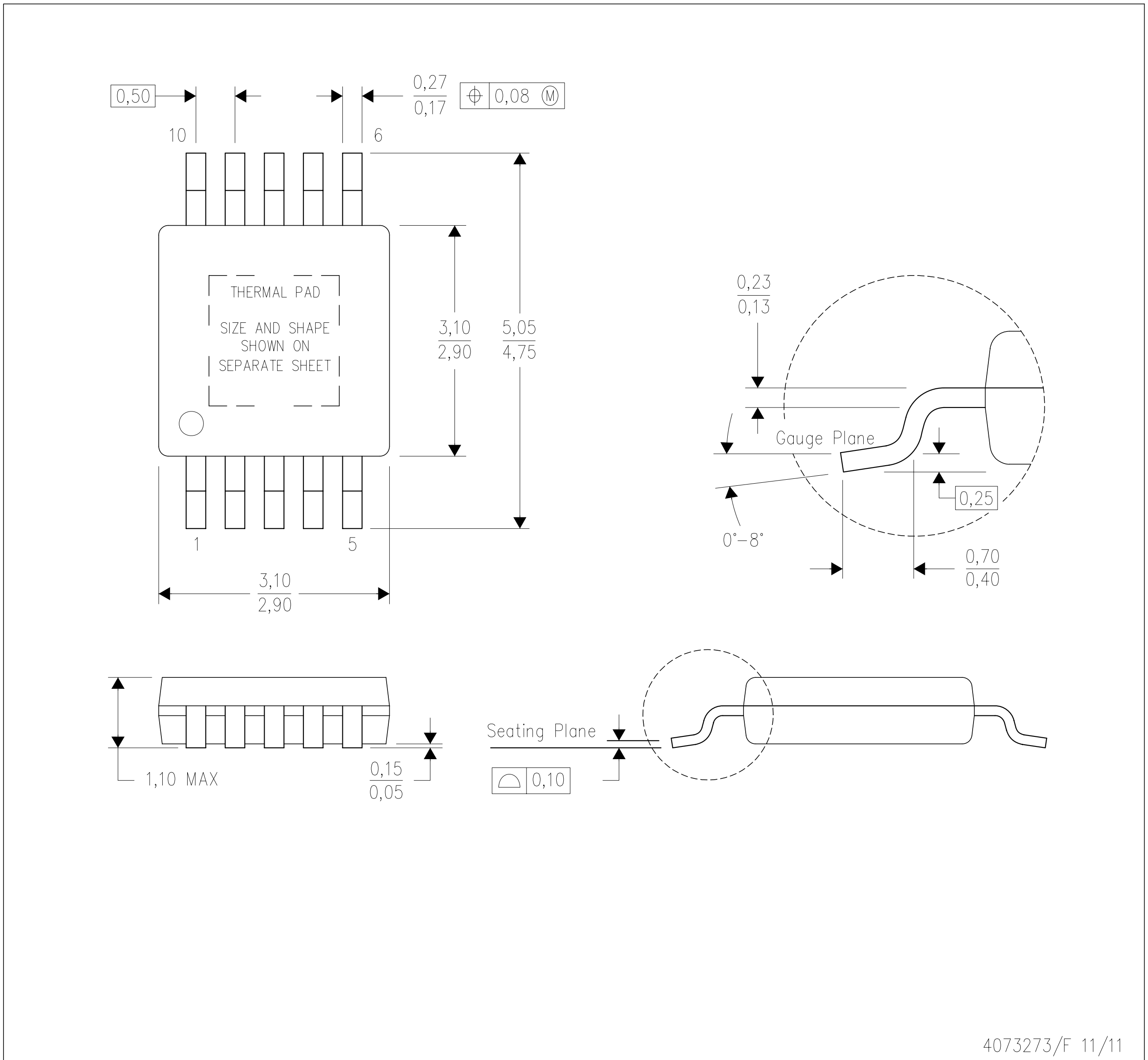
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGQ (S-PDSO-G10) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-187 variation BA-T.

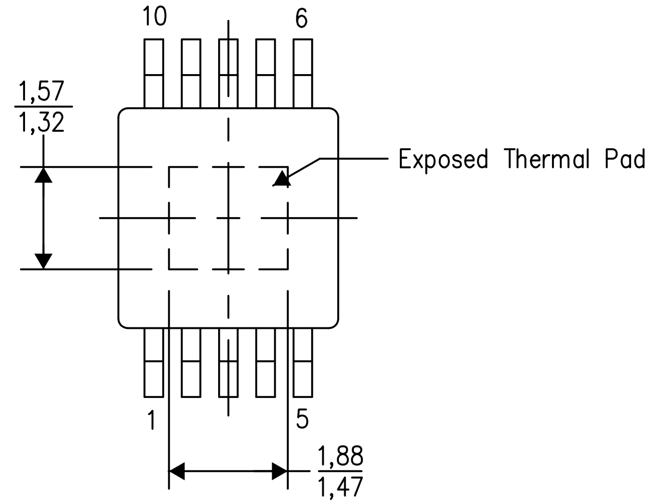
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

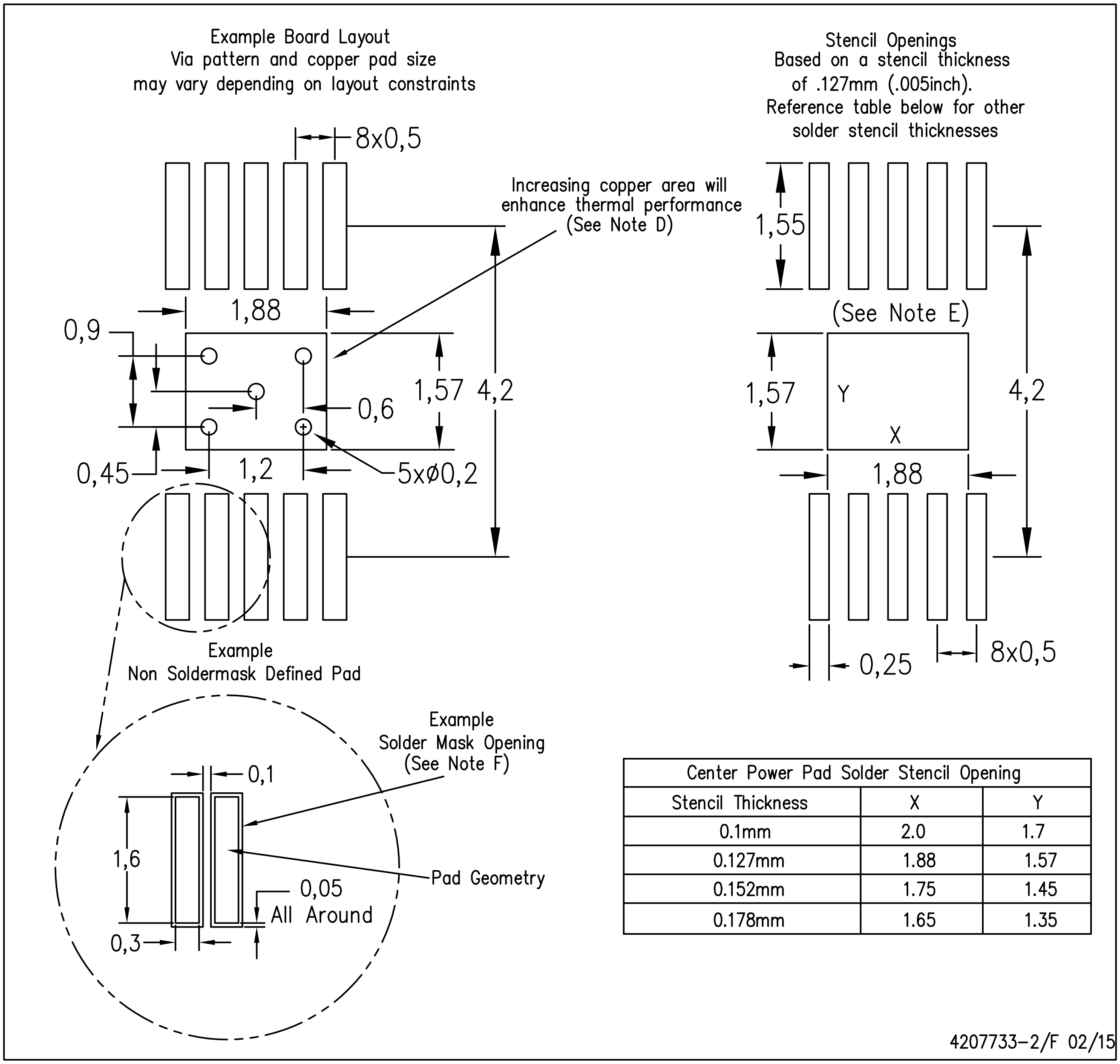
Exposed Thermal Pad Dimensions

4206324–2/H 12/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGQ (S-PDSO-G10) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.88	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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