

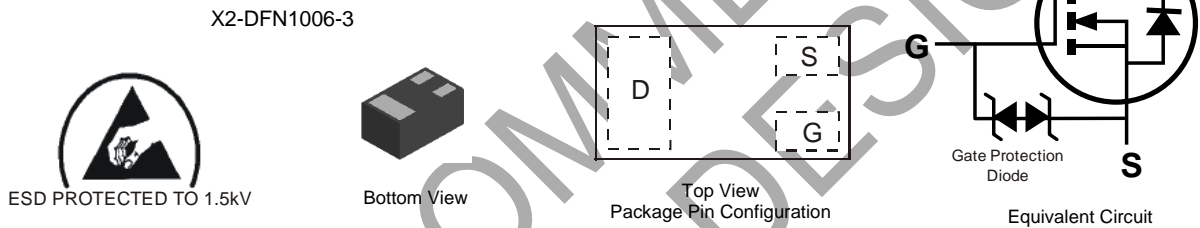
20V N-CHANNEL ENHANCEMENT MODE MOSFET

Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Ultra-Low Package Profile, 0.4mm Maximum Package Height
- ESD Protected up to 1.5kV
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 standards for High Reliability**

Mechanical Data

- Case: X2-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — NiPdAu over Copper Leadframe; Solderable per MIL-STD-202, Method 208 ^(e4)
- Weight: 0.001 grams (Approximate)



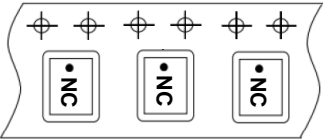
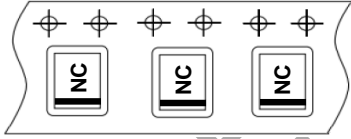

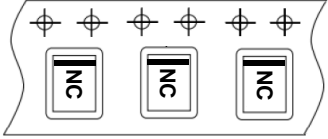

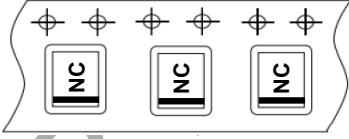


Ordering Information (Note 4)

Part Number	Marking	Reel Size (inches)	Tape Width (mm)	Tape Pitch (mm)	Quantity per Reel
DMN2400UFB4-7	NC	7	8	4	3,000
DMN2400UFB4-7R	NC	7	8	4	3,000
DMN2400UFB4-7B	NC	7	8	2	10,000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

<p>DMN2400UFB4-7</p>	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;">  <p>Top View Dot Denotes Drain Side</p> </div> <div style="text-align: center;"> <p>From date code 1527 (YYWW), this changes to:</p>  <p>Top View Bar Denotes Gate and Source Side</p> </div> </div> <div style="display: flex; justify-content: space-around; margin-top: 20px;">   </div>
<p>DMN2400UFB4-7R</p>	<div style="text-align: center;">  <p>Top View Bar Denotes Gate and Source Side</p> </div> <p style="text-align: right; margin-top: 10px;">NC = Part Marking Code</p> <div style="text-align: center; margin-top: 20px;">  </div>
<p>DMN2400UFB4-7B</p>	<div style="text-align: center;">  <p>Top View Bar Denotes Gate and Source Side</p> </div> <p style="text-align: right; margin-top: 10px;">NC = Part Marking Code</p> <div style="text-align: center; margin-top: 20px;">  </div>

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V _{DSS}	20	V	
Gate-Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current (Note 5) V _{GS} = 4.5V	I _D	Steady State T _A = +25°C	0.75	A
		T _A = +85°C	0.55	
Pulsed Drain Current (Notes 5 & 6)	I _{DM}	3	A	

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P _D	0.47	mW
Thermal Resistance, Junction to Ambient	R _{θJA}	258	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 PCB, with minimum recommended pad layout, single sided.
6. Device mounted on minimum recommended pad layout test board, 10μs pulse duty cycle = 1%.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	20	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	100 50	nA	V _{DS} = 20V, V _{GS} = 0V V _{DS} = 5V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±3V, V _{DS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±1.0	μA	V _{GS} = ±4.5V, V _{DS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±50	μA	V _{GS} = ±10V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	0.5	—	0.9	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	—	0.55	Ω	V _{GS} = 4.5V, I _D = 600mA
		—	—	0.75		V _{GS} = 2.5V, I _D = 500mA
		—	—	0.9		V _{GS} = 1.8V, I _D = 350mA
Forward Transfer Admittance	Y _{fs}	—	1.0	—	s	V _{DS} = 10V, I _D = 400mA
Diode Forward Voltage	V _{SD}	—	0.7	1.2	V	V _{GS} = 0V, I _S = 150mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	36.0	—	pF	V _{DS} = 16V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	5.7	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	4.2	—	pF	
Total Gate Charge	Q _g	—	0.5	—	nC	V _{GS} = 4.5V, V _{DS} = 10V, I _D = 250mA
Gate-Source Charge	Q _{gs}	—	0.07	—	nC	
Gate-Drain Charge	Q _{gd}	—	0.1	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	4.11	—	ns	V _{DD} = 10V, V _{GS} = 4.5V, R _L = 47Ω, R _g = 10Ω, I _D = 200mA
Turn-On Rise Time	t _R	—	3.82	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	14.8	—	ns	
Turn-Off Fall Time	t _F	—	9.6	—	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

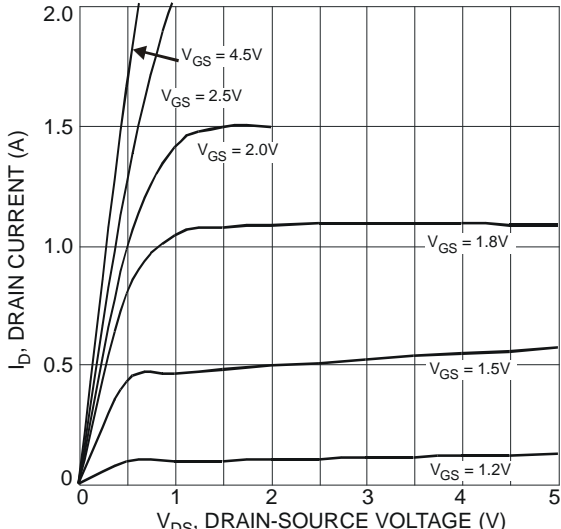


Fig. 1 Typical Output Characteristics

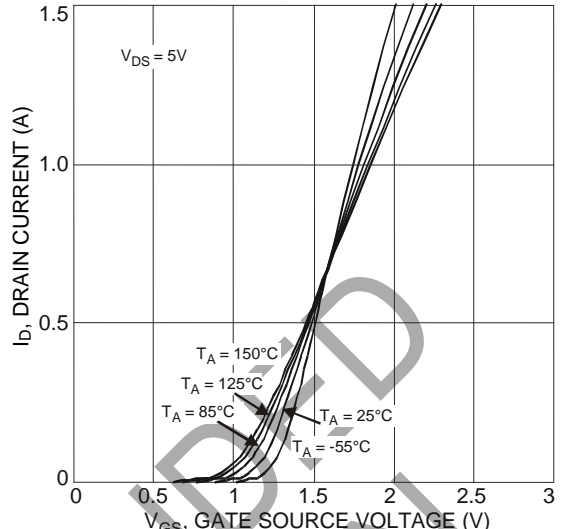


Fig. 2 Typical Transfer Characteristics

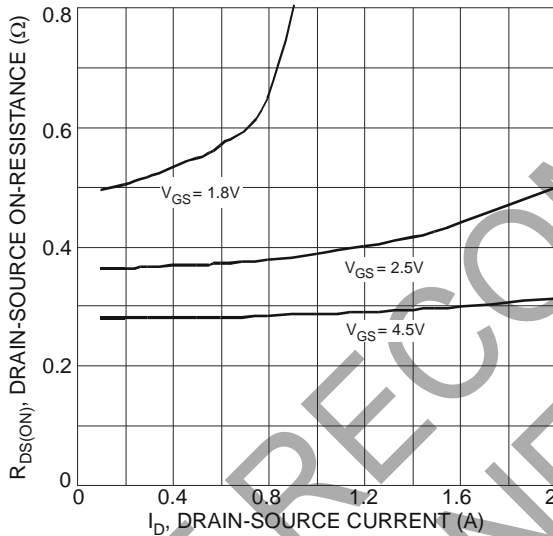


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

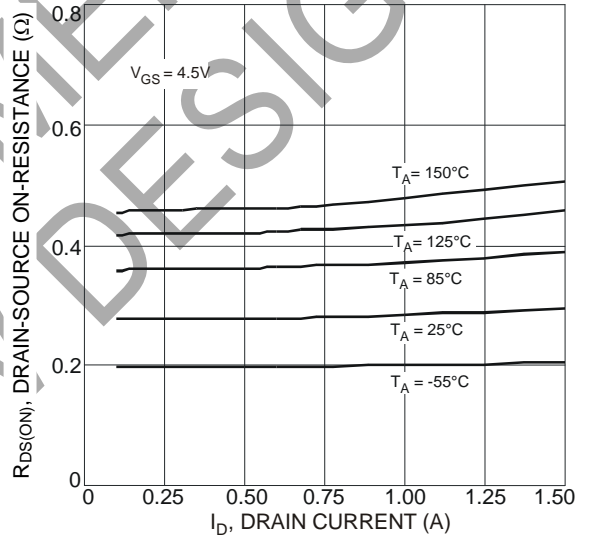


Fig. 4 Typical Drain-Source On-Resistance vs. Drain Current and Temperature

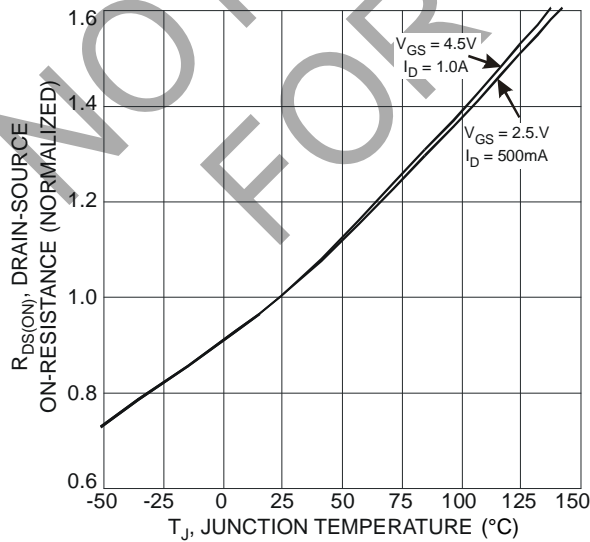


Fig. 5 On-Resistance Variation with Temperature

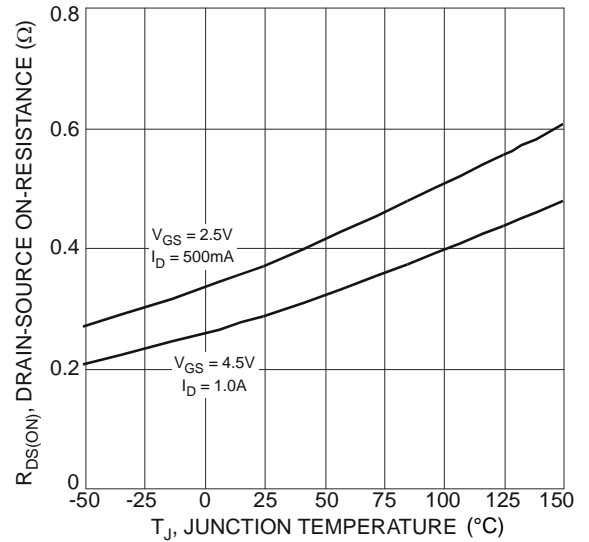


Fig. 6 On-Resistance Variation with Temperature

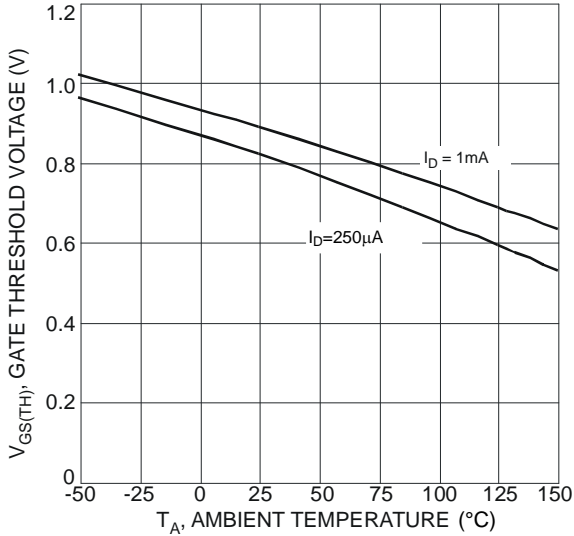


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

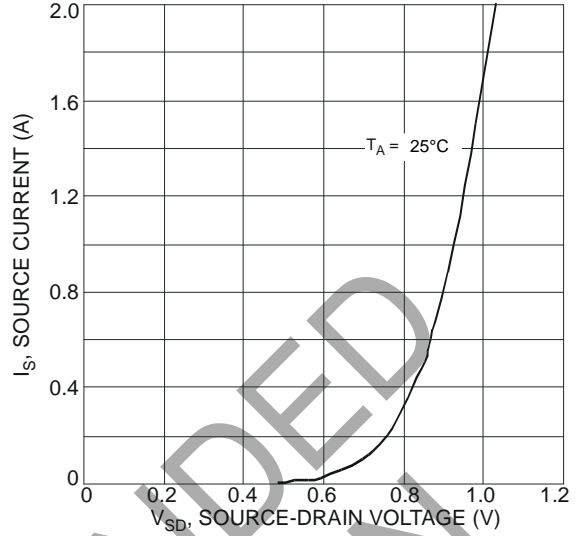


Fig. 8 Diode Forward Voltage vs. Current

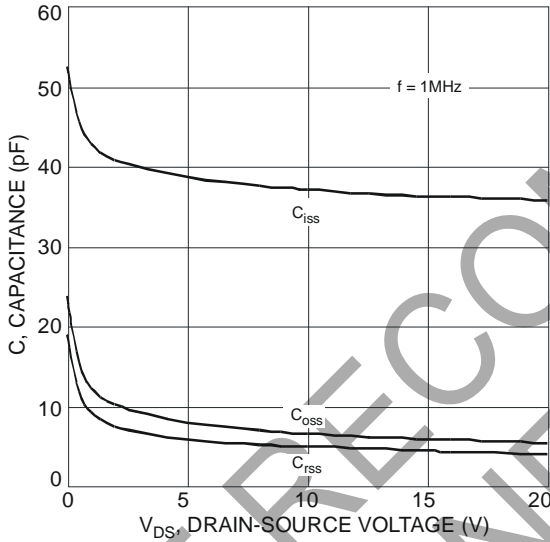


Fig. 9 Typical Capacitance

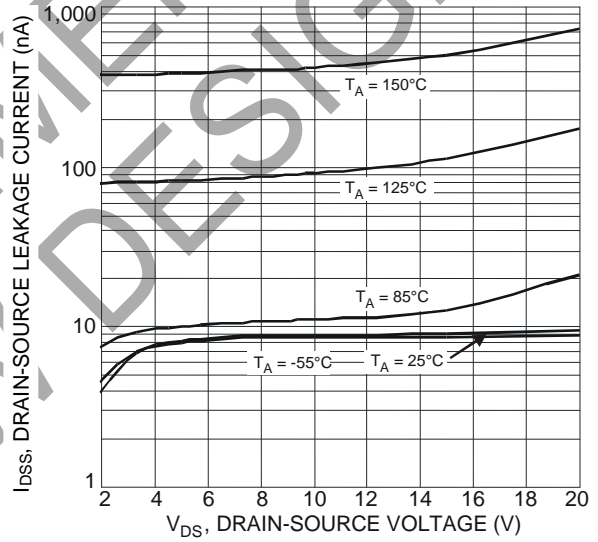


Fig. 10 Typical Drain-Source Leakage Current vs. Drain-Source Voltage

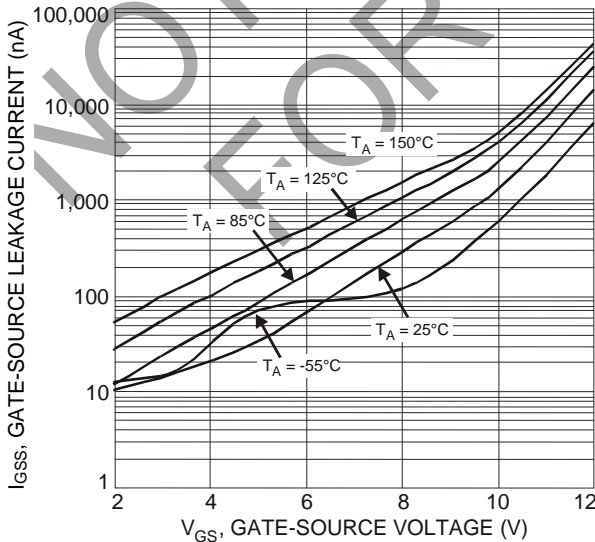


Fig. 11 Typical Gate-Source Leakage Current vs. Gate-Source Voltage

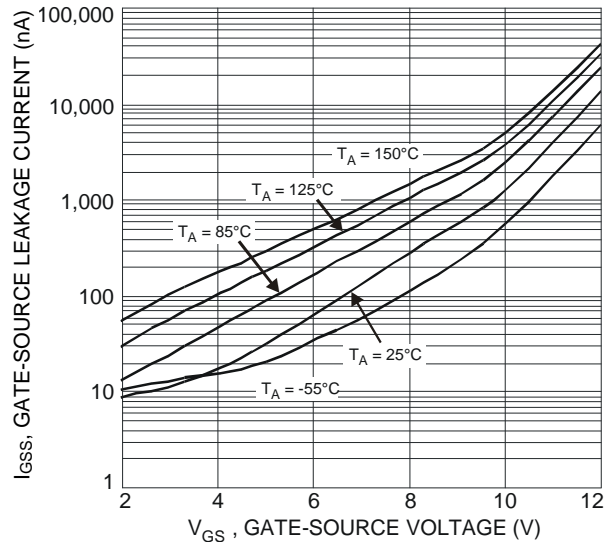


Fig. 12 Typical Gate-Source Leakage Current vs. Gate-Source Voltage

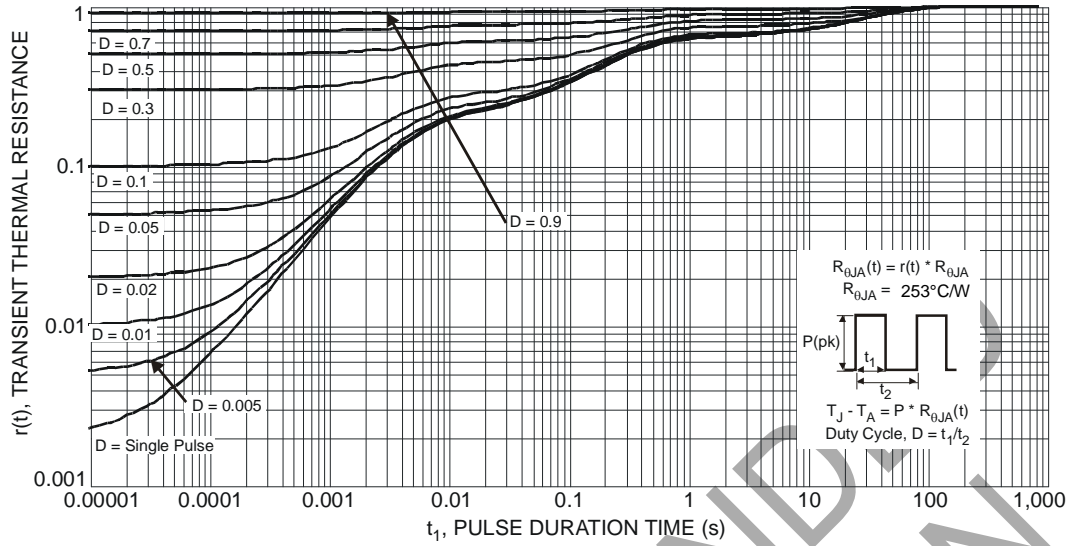


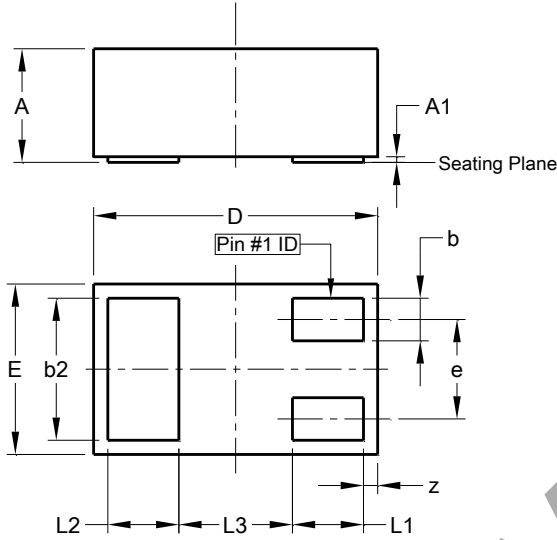
Fig. 13 Transient Thermal Response

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Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1006-3

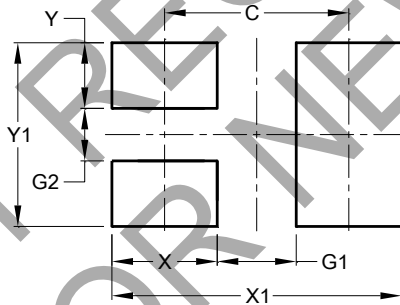


X2-DFN1006-3			
Dim	Min	Max	Typ
A	-	0.40	-
A1	0.00	0.05	0.03
b	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.05	1.00
E	0.55	0.65	0.60
e	-	-	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	-	-	0.40
z	0.02	0.08	0.05
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

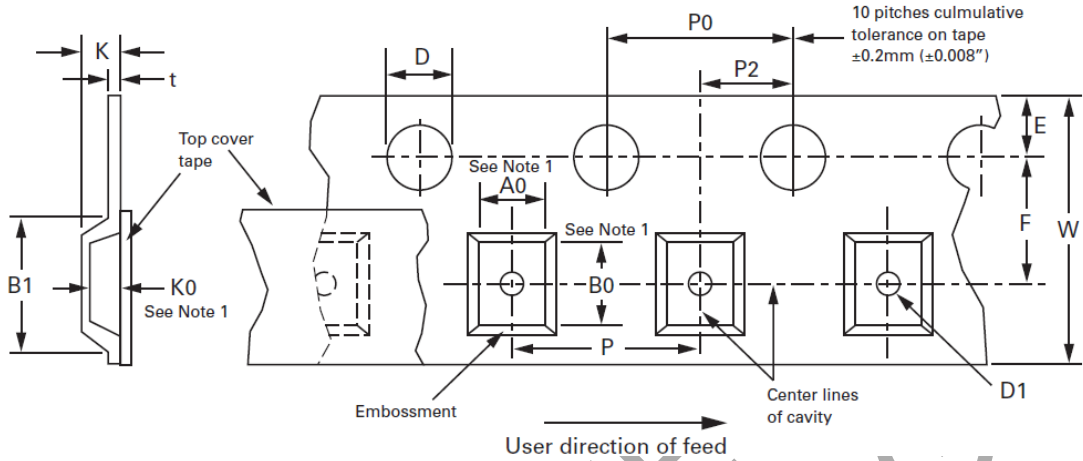
X2-DFN1006-3



Dimensions	Value (in mm)
C	0.70
G1	0.30
G2	0.20
X	0.40
X1	1.10
Y	0.25
Y1	0.70

Tape Information

EMBOSSED CARRIER TAPE SPECIFICATIONS



8, 12, 16, 24mm EMBOSSED TAPE DIMENSIONS IN mm						
Tape Size	D	E	P _o	t _{max}	A _o B _o K _o	Constant Dimensions
8mm	1.50 +0.10 -0.0	1.75 ± 0.10	4.0 ± 0.10	0.400	See Note 9	

Tape Size	B1 max	D1 min	F	K max	P2	R min	W	Package Type
8mm	4.5	0.35	3.5 ± 0.05	2.4	2.0 ± 0.05	25	8.0 ± 0.30	Refer to 8mm Device Tape Orientation Table

P					
Tape Size	2.0 ± 0.05	4.0 ± 0.10	8.0 ± 0.10	12.0 ± 0.10	16.0 ± 0.10
8mm	DFN1006 (-7B)	DFN1006 (-7) DFN1006 (-7R)	—	—	—

Note: 9. A_o B_o K_o are determined by component size.

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