DDR4 SDRAM UDIMM

CT8G4DFS8### - 8GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin, registered dual in-line, memory module (UDIMM)
- Fast data transfer rates: PC4-2666, PC4-2400, or PC4-2133
- 8GB (1 Gig x 64)
- V_{DD} = 1.2V (NOM)
- V_{PP} = 2.5V (NOM)
- V_{DDSPD} = 2.2–3.6V (NOM)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die V_{REFDQ} generation and calibration
- Single-rank
- On-board I^2 serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command and address bus

Figure 1: 288-Pin UDIMM (MO-309 R/C-A1)

Module height: 31.25mm (1.23in)

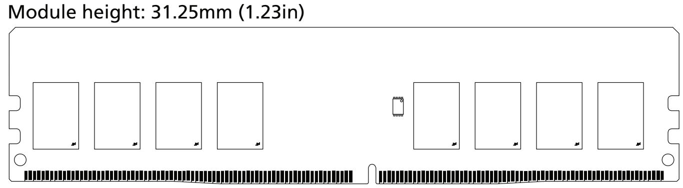


Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)											^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL= 20, CL= 19	CL = 18	CL = 17	CL = 16	CL = 15	CL = 14	CL = 13	CL = 12	CL = 11	CL = 10	CL = 9			
266	PC4-2666	2666	2666	2400	2133	2133	1866	1866	1600	–	1333	–	13.5	13.5	45.5
24A	PC4-2400	–	2400	2400	2133	2133	1866	1866	1600	1600	1333	–	14.16	14.16	46.16
213	PC4-2133	–	–	–	2133	2133	1866	1866	1600	1600	1600	1333	13.5	13.5	46.5

Table 2: Addressing

Parameter	8GB
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	8Gb (1 Gig x 8), 16 banks
Module rank address	CS0_n

Table 3: Part Numbers and Timing Parameters - 8GB Modules

Base device:MT40A1G8[1] 8Gb DDR4 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
CT8G4DFS8266.z8xy	8GB	1 Gig x 64	21.3 GB/s	0.75ns/2666MT/s	19-19-19
CT8G4DFS824A.z8xy	8GB	1 Gig x 64	19.2 GB/s	0.83ns/2400 MT/s	17-17-17
CT8G4DFS8213.z8xy	8GB	1 Gig x 64	17.0 GB/s	0.93ns/2133 MT/s	15-15-15

Notes:
1. The data sheet for the base device can be found on by contacting your Micron Consumer Products Group Sales Representative.
2. All part numbers end with a code (not shown) that designates component revisions. Consult factory for current revision codes. Example: CT8G4DFS824A.z8xy, where z is the mark on the DRAM (not present or M is Micron, and C is CPG) and x and y are for component revisions and traceability.

Pin Assignments

Table 4: Pin Assignments

288-Pin DDR4 UDIMM Front								288-Pin DDR4 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NC	37	V_{SS}	73	V_{DD}	109	V_{SS}	145	NC	181	DQ29	217	V_{DD}	253	DQ41
2	V_{SS}	38	DQ24	74	CK0_t	110	DM5_n/ DBI5_n, NC	146	V_{REFCA}	182	V_{SS}	218	CK1_t	254	V_{SS}
3	DQ4	39	V_{SS}	75	CK0_c	111	NC	147	V_{SS}	183	DQ25	219	CK1_c	255	DQS5_c
4	V_{SS}	40	DM3_n/ DBI3_n, NC	76	V_{DD}	112	V_{SS}	148	DQ5	184	V_{SS}	220	V_{DD}	256	DQS5_t
5	DQ0	41	NC	77	V_{TT}	113	DQ46	149	V_{SS}	185	DQS3_c	221	V_{TT}	257	V_{SS}
6	V_{SS}	42	V_{SS}	78	EVENT_n, NF	114	V_{SS}	150	DQ1	186	DQS3_t	222	PARITY	258	DQ47
7	DM0_n/ DBI0_n, NC	43	DQ30	79	A0	115	DQ42	151	V_{SS}	187	V_{SS}	223	V_{DD}	259	V_{SS}
8	NC	44	V_{SS}	80	V_{DD}	116	V_{SS}	152	DQS0_c	188	DQ31	224	BA1	260	DQ43
9	V_{SS}	45	DQ26	81	BA0	117	DQ52	153	DQS0_t	189	V_{SS}	225	A10/AP	261	V_{SS}
10	DQ6	46	V_{SS}	82	RAS_n/ A16	118	V_{SS}	154	V_{SS}	190	DQ27	226	V_{DD}	262	DQ53
11	V_{SS}	47	CB4/ NC	83	V_{DD}	119	DQ48	155	DQ7	191	V_{SS}	227	NC	263	V_{SS}
12	DQ2	48	V_{SS}	84	CS0_n	120	V_{SS}	156	V_{SS}	192	CB5/ NC	228	WE_n/ A14	264	DQ49
13	V_{SS}	49	CB0/ NC	85	V_{DD}	121	DM6_n/ DBI6_n, NC	157	DQ3	193	V_{SS}	229	V_{DD}	265	V_{SS}
14	DQ12	50	V_{SS}	86	CAS_n/ A15	122	NC	158	V_{SS}	194	CB1, NC	230	NC	266	DQS6_c
15	V_{SS}	51	DM8_n/ DBI8_n, NC	87	ODT0	123	V_{SS}	159	DQ13	195	V_{SS}	231	V_{DD}	267	DQS6_t
16	DQ8	52	NC	88	V_{DD}	124	DQ54	160	V_{SS}	196	DQS8_c	232	A13	268	V_{SS}
17	V_{SS}	53	V_{SS}	89	CS1_n	125	V_{SS}	161	DQ9	197	DQS8_t	233	V_{DD}	269	DQ55
18	DMI_n/ DBI1_n, NC	54	CB6/ DBI8_n, NC	90	V_{DD}	126	DQ50	162	V_{SS}	198	V_{SS}	234	NC	270	V_{SS}
19	NC	55	V_{SS}	91	ODT1	127	V_{SS}	163	DQS1_c	199	CB7, NC	235	NC	271	DQ51
20	V_{SS}	56	CB2/ NC	92	V_{DD}	128	DQ60	164	DQS1_t	200	V_{SS}	236	V_{DD}	272	V_{SS}
21	DQ14	57	V_{SS}	93	NC	129	V_{SS}	165	V_{SS}	201	CB3, NC	237	NC	273	DQ61
22	V_{SS}	58	RESET_n	94	V_{SS}	130	DQ56	166	DQ15	202	V_{SS}	238	SA2	274	V_{SS}
23	DQ10	59	V_{DD}	95	DQ36	131	V_{SS}	167	V_{SS}	203	CKE1	239	V_{SS}	275	DQ57
24	V_{SS}	60	CKE0	96	V_{SS}	132	DM7_n/ DBI7_n, NC	168	DQ11	204	V_{DD}	240	DQ37	276	V_{SS}
25	DQ20	61	V_{DD}	97	DQ32	133	NC	169	V_{SS}	205	NC	241	V_{SS}	277	DQS7_c
26	V_{SS}	62	ACT_n	98	V_{SS}	134	V_{SS}	170	DQ21	206	V_{DD}	242	DQ33	278	DQS7_t
27	DQ16	63	BG0	99	DM4_n/ DBI4_n, NC	135	DQ62	171	V_{SS}	207	BG1	243	V_{SS}	279	V_{SS}

Pin Assignments

Table 4: Pin Assignments (Continued)

288-Pin DDR4 UDIMM Front								288-Pin DDR4 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
28	V_{SS}	64	V_{DD}	100	NC	136	V_{SS}	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DM2_n/ DBI2_n, NC	65	A12/BC_n	101	V_{SS}	137	DQ58	173	V_{SS}	209	V_{DD}	245	DQS4_t	281	V_{SS}
30	NC	66	A9	102	DQ38	138	V_{SS}	174	DQS2_c	210	A11	246	V_{SS}	282	DQ59
31	V_{SS}	67	V_{DD}	103	V_{SS}	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	V_{SS}
32	DQ22	68	A8	104	DQ34	140	SA1	176	V_{SS}	212	V_{DD}	248	V_{SS}	284	V_{DDSPD}
33	V_{SS}	69	A6	105	V_{SS}	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	V_{DD}	106	DQ44	142	V_{PP}	178	V_{SS}	214	A4	250	V_{SS}	286	V_{PP}
35	V_{SS}	71	A3	107	V_{SS}	143	V_{PP}	179	DQ19	215	V_{DD}	251	DQ45	287	V_{PP}
36	DQ28	72	A1	108	DQ40	144	NC	180	V_{SS}	216	A2	252	V_{SS}	288	V_{PP}

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 UDIMM, RDIMM, SODIMM and LRDIMM modules. All pins listed may not be supported on the module defined in this data sheet. See functional block diagram specific to this module to review all pins utilized on this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation (HIGH = Auto precharge; LOW = No auto precharge). A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst Chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = No burst chop; LOW = Burst-chopped). See the Command Truth Table in DDR4 component data sheet for more information.
ACT_n	Input	**Command input:** ACT_n defines the activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as row address A16, A15, and A14. See the Command Truth Table in DDR4 component data sheet for more information.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define which bank group a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16 based SDRAMs only has BG0.
C0, C1, C2 (RDIMM/ LRDIMM Only)	Input	**Chip ID:** These inputs are used only when devices are stacked, that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using though-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which use CS1_n, CKE1, and ODT1 to control the second die. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave)-type configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

Table 5: Pin Descriptions (Continued)

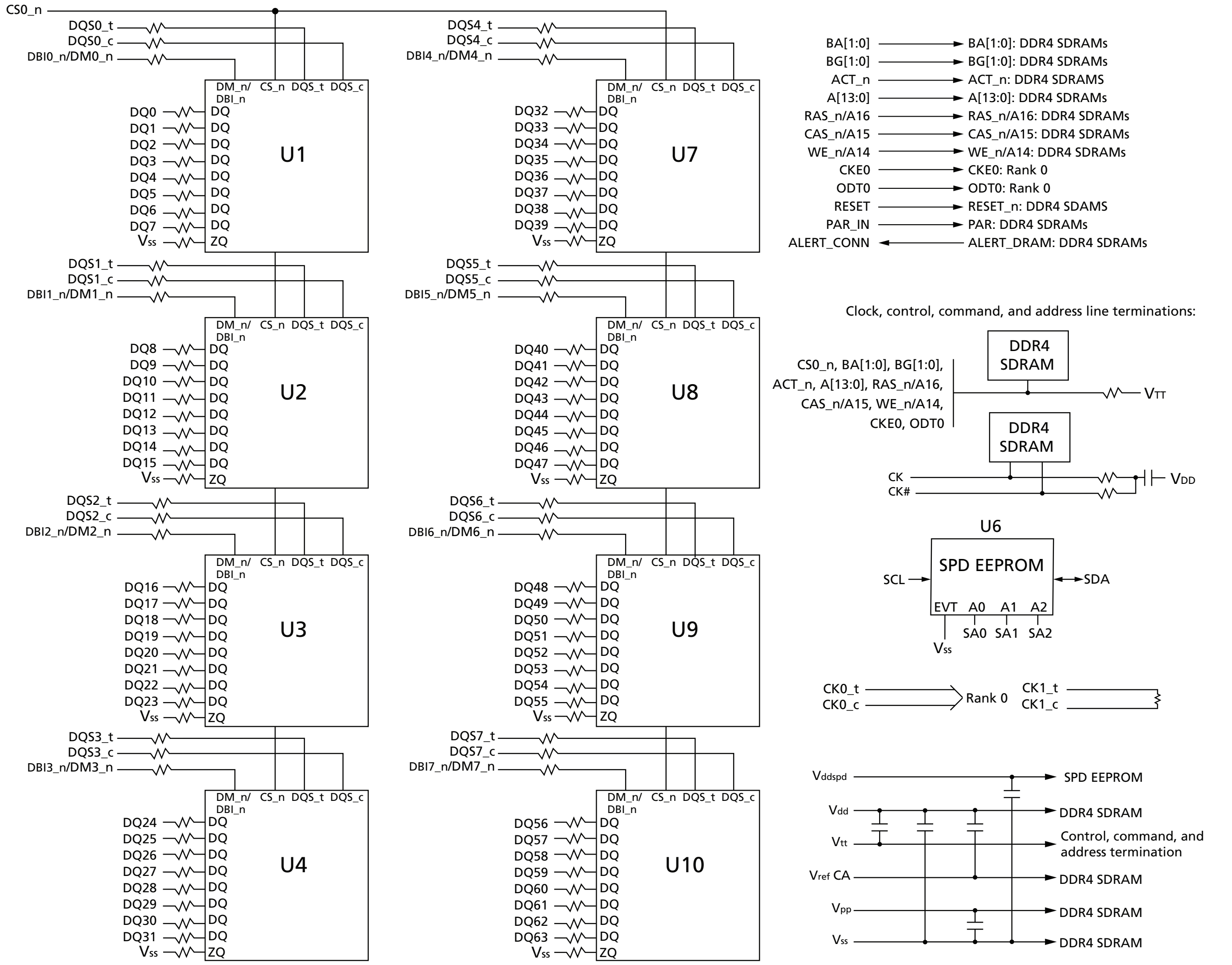
Symbol	Type	Description
CKEx	Input	**Clock enable:** CKE HIGH activates, and CKE LOW deactivates, the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be held HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code. (CS2_n and CS3_n are not used on UDIMMs).
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When ODT is enabled, on-die termination (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time with command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered. Those pins have multifunction. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in the command truth table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW; inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and Check Bit input/output :** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, then CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
DM_n/DBI_n/ TDQS_t(DMU_n ,DBI U_n),(DML_n/ DBIl_n)	I/O	**Input Data Mask and Data Bus Inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. (TDQS is not valid for UDIMMs.)
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/ TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a singleended data strobe.
ALERT_n	Output	**Alert output:** Possesses multifunctions such as CRC error flag and command and address parity error flag as output signal. If there is a CRC error, then ALERT_n goes LOW for the period time interval and returns HIGH. If there is error in command address parity check, then ALERT_n goes LOW until on-going DRAM internal recovery transaction is complete. During connectivity test mode this pin functions as an input. Using this signal or not is dependent on the system. If not connected as signal, ALERT_n pin must be connected to V_{DD} on DIMM.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.
TDQS_t TDQS_c (x8 DRAM based RDIMM only)	Output	**Termination data strobe:** TDQS_t and TDQS_c are not valid for UDIMMs. When enabled via the mode register, the SDRAM enable the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/ disabled by mode register settings. For further information about TDQS, refer to DDR4 DRAM data sheet.
V_{DD}	Supply	**Module Power supply:** 1.2V (typical)
V_{PP}	Supply	**DRAM activating power supply:** 2.5V -0.125V / +0.250V
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{TT}	Supply	Power supply for termination of address, command, and control, $V_{DD}/2$.
V_{DDSPD}	Supply	Power supply used to power the I^2C bus used for SPD.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.

Functional Block Diagram

Figure 2: Functional Block Diagram



Notes: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and outpu driver.

General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with two or four internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM devices have four internal bank groups consisting of four memory banks each, providing a total of 16 banks. 16-bit-wide DDR4 SDRAM devices have two internal bank groups consisting of four memory banks each, providing a total of eight banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8n-bitwide, four-clock data transfer at the internal DRAM core and eight corresponding n-bitwide, one-half-clock-cycle data transfers at the I/O pins.

DDR4 modules use two sets of differential signals: DQS_t, DQS_c to capture data and CK_t and CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

FLy-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

Address Mapping to DRAM

Address Mirroring

To achieve optimum routing of the address bus on DDR4 multi rank modules, the address bus will be wired as shown in the table below, or mirrored. For quad rank modules, ranks 1 and 3 are mirrored and ranks 0 and 2 are non-mirrored. Highlighted address pins have no secondary functions allowing for normal operation when cros wired. Data is still read from the same address it was written. However, Load Mode operations require a specific address. This requires the controller to accommodate for a rank that is "mirrored." Systems may reference DDR4 SPD to determine if the module has mirroring implemented or not. See the JEDEC DDR4 SPD specification for more details.

Table 6: Address Mirroring

Edge Connector Pin	DRAM Pin, Non-mirrored	DRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
A10	A10	A10
A11	A11	A13
A13	A13	A11
A12	A12	A12
A14	A14	A14
A15	A15	A15
A16	A16	A16
A17	A17	A17
BA0	BA0	BA1
BA1	BA1	BA0
BG0	BG0	BG1
BG1	BG1	BG0

SPD EEPROM Operation

DDR4 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 512-byte JEDEC JC-42.4 compliant EEPROM that is segregated into four, 128-byte, write protectable blocks. The SPD content is aligned with these blocks as shown in the table below.

Block	Range		Discription
0	0–127	000h–07Fh	Configuration and DRAM Parameters
1	128 - 255	080h–0FFh	Module Parameters
2	256 -319	100h–13Fh	Reserved - All bytes coded as 0x00
	320 - 383	140h–17Fh	Manufacturing Information
3	384 - 511	180h–1FFh	End User Programmable

The first 384 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR4 SDRAM Modules." The remaining 128 bytes of storage are available for use by the customer.

The EEPROM resides on a two-wire I^2C serial interface and is not integrated with the memory bus in any way. It operates as a slave device in the I^2C bus protocol, with all operations synchronized by the serial clock. Transfer rates of up to 1 MHz are achievable at 2.2–3.6V.

Micron implements reversible software write protection on DDR4 SDRAM-based modules. This prevents the lower 384 bytes (bytes 0–383) from being inadvertently programmed or corrupted. The upper 128 bytes remain available for customer use and unprotected.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.5	V	1
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}	–0.4	1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.4	3.0	V	2
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.5	V	

Table 8: Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage command/address bus	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	3
I_{VTT}	Termination reference current from V_{TT}	–750	–	+750	mA	
V_{TT}	Termination reference voltage (DC) – command/ address bus	0.49 x V_{DD} - 20mV	0.5 x V_{DD}	0.51 x V_{DD} + 20mV	V	4
I_I	Input leakage current; Any input excluding ZQ; 0V < V_{IN} < 1.1V	–2.0	–	2.0	µA	5
$I_{I/O}$	DQ leakage; 0V < V_{IN} < V_{DD}	–4.0	–	4.0	µA	5
I_I	Input leakage current; ZQ	–3.0	–	3.0	µA	5,6
I_{OZpd}	Output leakage current; V_{OUT} = V_{DD}; DQ are disabled	–	–	5.0	µA	
I_{OZpu}	Output leakage current; V_{OUT} = V_{SS}; DQ and ODT are disabled; ODT is disabled with ODT input HIGH	–	–	5.0	µA	
I_{VREFCA}	V_{REFCA} leakage; V_{REFCA} = V_{DD}/2 (After DRAM is initialized)	–2	–	+2	µA	5

Notes:
1. V_{DDQ} tracks with V_{DD}; V_{DDQ} and V_{DD} are tied together.
2. V_{PP} must be greater than or equal to V_{DD} at all times.
3. V_{REFCA} must not be greater than 0.6 × V_{DD}. When V_{DD} is less than 500mV, V_{REF} may be less than or equal to 300mV.
4. V_{TT} termination voltages in excess of specification limit will adversely affect command and address signals' voltage margins, and reduce timing margins.
5. Multiply by number of DRAM die on module.
6. Tied to ground. Not connected to edge connector.

Table 9: Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
T_C	Commercial operating case temperature	0 to +85	°C	1, 2, 3
T_C		>85 to +95	°C	1, 2, 3, 4
T_{OPER}	Normal operating temperature range	0 to +85	°C	5, 7
T_{OPER}	Extended temperature operating range (optional)	>85 to 95	°C	5, 7
T_{STG}	Non-operating storage temperature	-55 to 100	°C	6
RH_{STG}	Non-operating Storage Relative Humidity (non-condensing)	5 to 95	%	
NA	Change Rate of Storage Temperature	20	°C/hour	

Notes:
1. MAX operating case temperature. T_C is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9μs interval refresh rate.
5. The refresh rate is required to double when 85°C < T_{OPER} ≤ 95°C.
6. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.
7. For additional information, refer to technical note TN-00-08: "Thermal Applications" available at micron.com.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR4 component data sheets. Component specifications are available on Micron's web site. Module speed grades correlate with component speed grades, as shown below.

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level.

Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the edge connector of the module, not the DRAM. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 10: DDR4 I_{DD} Specifications and Conditions - 8GB

Values are for the MT40A1G8 DDR4 SDRAM only and are computed from values specified in the 8Gb (1 Gig x 8) component data sheet

Parameter	Symbol	2666	2400	2133	Units
One bank ACTIVATE-PRECHARGE current	I_{DD0}	520	480	440	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I_{PP} current	I_{PP0}	24	24	24	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{DD1}	640	600	560	mA
Precharge standby current	I_{DD2N}	440	400	360	mA
Precharge standby ODT current	I_{DD2NT}	520	480	440	mA
Precharge power-down current	I_{DD2P}	280	240	200	mA
Precharge quiet standby current	I_{DD2Q}	400	360	360	mA
Active standby current	I_{DD3N}	480	440	440	mA
Active standby I_{PP} current	I_{PP3N}	24	24	24	mA
Active power-down current	I_{DD3P}	320	320	280	mA
Burst read current	I_{DD4R}	1400	1200	1200	mA
Burst read IDDQ current	I_{DDQ4R}	560	520	480	mA
Burst write current	I_{DD4W}	1400	1280	1200	mA
Burst refresh current (1x REF)	I_{DD5B}	1800	1800	1800	mA
Burst refresh I_{PP} current (1 x REF)	I_{PP5B}	240	240	240	mA
Self refresh current: Normal temperature range (0°C to +85°C)	I_{DD6N}	240	240	240	mA
Self refresh current: Extended temperature range (0°C to +95°C)	I_{DD6E}	280	280	280	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	I_{DD6R}	200	200	200	mA
Auto self refresh current (25°C)	I_{DD6A}	160	160	160	mA
Auto self refresh current (45°C)	I_{DD6A}	200	200	200	mA
Auto self refresh current (75°C)	I_{DD6A}	280	280	280	mA
Bank interleave read current	I_{DD7}	1720	1640	1600	mA
Bank interleave read I_{PP} current	I_{PP7}	120	120	120	mA
Maximum power-down current	I_{DD8}	160	160	160	mA

SPD EEPROM Operating Conditions

For the latest SPD data contact your Micron Consumer Products Group Sales Representative.

Table 11: Serial Presence-Detect EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.2	3.6	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.5	V_{DDSPD} + 0.3	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} + 0.7	V_{DDSPD} + 0.5	V
Output low voltage: 3 mA sink current V_{DDSPD} >2V	V_{OL}	–	0.4	V
Input leakage current: (SCL, SDA) V_{IN} = V_{DDSPD} or V_{SSSPD}	I_{LI}	–	±5	µA
Output leakage current: V_{OUT} = V_{DDSPD} or V_{SSSPD}, SDA in High-Z	I_{LO}	–	±5	µA

Notes: 1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.
2. All voltages referenced to V_{DDSPD}.

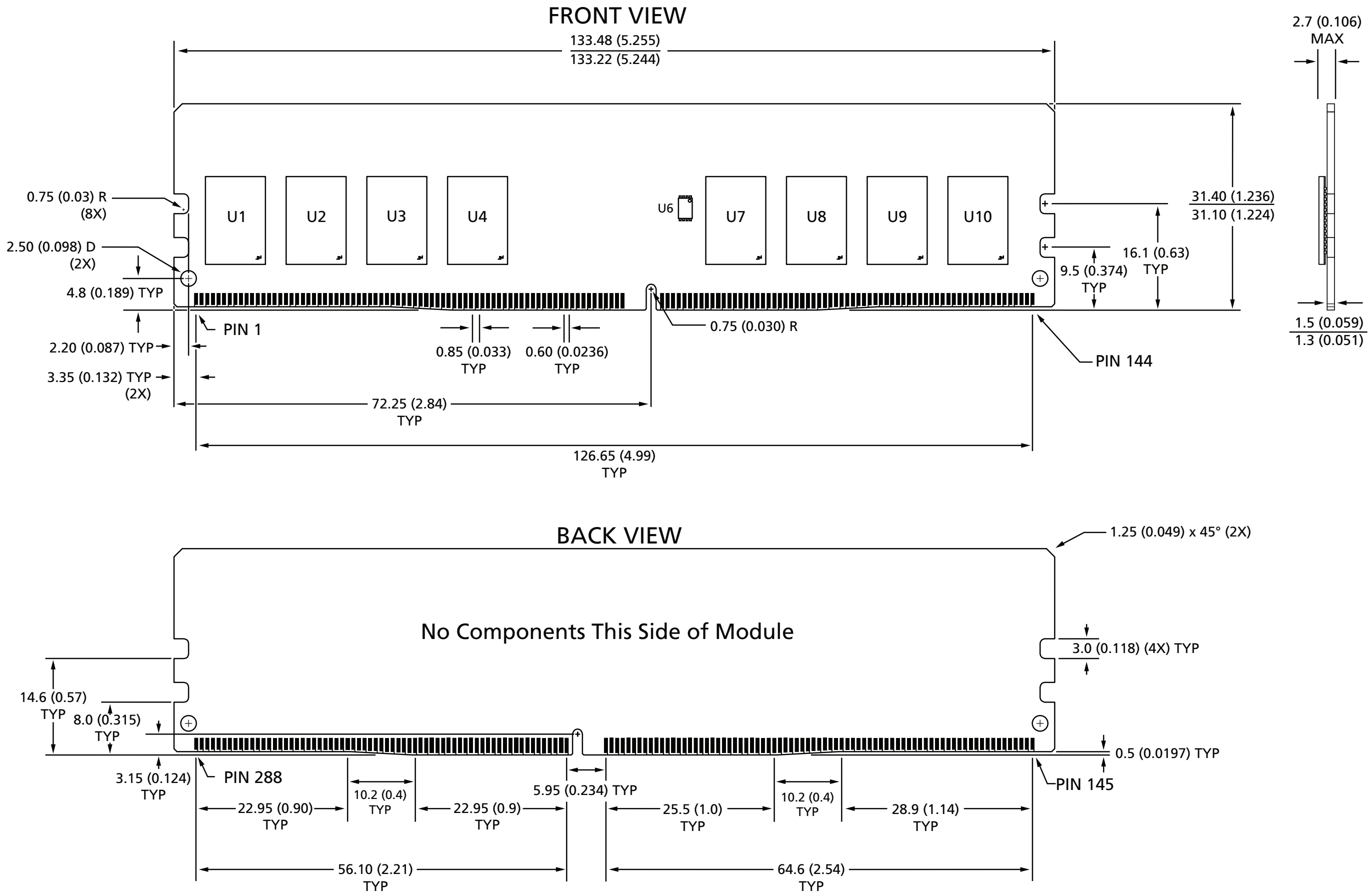
Table 12: Serial Presence-Detect EEPROM Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	^{t}SCL	10	1000	kHz
Clock pulse width high time	$^{t}HIGH$	260	–	ns
Clock pulse width low time	^{t}LOW	500	–	ns
Detect Clock Low Timeout	$^{t}TIMEOUT$	25	35	ms
SDA rise time	^{t}R	–	120	ns
SDA fall time	^{t}F	–	120	ns
Data-in setup time	$^{t}SU:DAT$	50	–	ns
Data-in hold time	$^{t}HD:DI$	0	–	ns
Data-out hold time	$^{t}HD:DAT$	0	350	ns
Start condition setup time	$^{t}SU:STA$	260	–	ns
Start condition hold time	$^{t}HD:STA$	260	–	ns
Stop condition setup time	$^{t}SU:STO$	260	–	ns
Time the bus must be free before a new transition can start	^{t}BUF	500	–	ns
WRITE time	^{t}W	–	5	ms
Warm power cycle time off	$^{t}POFF$	1	–	ms
Time from power on to first command	$^{t}INIT$	10	–	ms

Notes: 1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.

Module Dimensions

Figure 3: 288-Pin DDR4 UDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only and showing one possible configuration.

3475 E. Commercial Ct., Meridian, ID 83642, Tel: 208-363-5500, Internet:
http://www.crucial.com