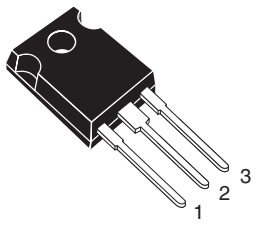
# STW45NM50

## N-channel 550 V @ $T_J$max, 0.08 Ω, 45 A, TO-247 MDmesh™ Power MOSFET

## Features

| Type | $V_{DSS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STW45NM50FD | 500 V | < 0.1 Ω | 45 A |

- 100% avalanche tested
- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance




**TO-247**

## Application

- Switching applications

## Description

The MDmesh™ is a new revolutionary Power MOSFET technology that associates the Multiple Drain process with the company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competitor's products.

**Figure 1. Internal schematic diagram**

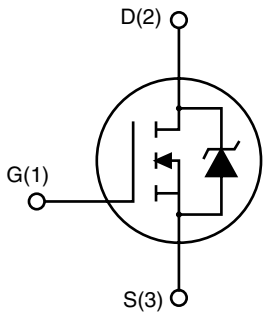



**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STW45NM50 | W45NM50 | TO-247 | Tube |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ± 30 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 45 | A |
| $I_D$ | Drain current (continuous) at $T_C$=100 °C | 28.4 | A |
| $I_{DM}$(1) | Drain current (pulsed) | 180 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 417 | W |
| | Derating factor | 2.08 | W/°C |
| dv/dt(2) | Peak diode recovery voltage slope | 15 | V/ns |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature | -65 to 150 | °C |

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 45$ A, di/dt $\leq$ 400 A/µs, $V_{DD} = 80\%V_{(BR)DSS}$

**Table 3. Thermal resistance**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 0.3 | °C/W |
| $R_{thj\text{-}a}$ | Thermal resistance junction-ambient max | 30 | °C/W |
| $T_l$ | Maximum lead temperature for soldering purpose | 300 | °C |

**Table 4. Avalanche data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max) | 20 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D = I_{AR}$, $V_{DD}$ = 50 V) | 810 | mJ |

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified)

**Table 5. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 250 µA, $V_{GS}$= 0 | 500 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating,<br>$V_{DS}$ = Max rating @125 °C | | | 10<br>100 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 30 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$= $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$= 10 V, $I_D$= 22.5 A | | 0.08 | 0.1 | Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DS}$ >$I_{D(on)}$ x $R_{DS(on)max}$<br>$I_D$ = 22.5 A | - | 20 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ =25 V, f=1 MHz, $V_{GS}$=0 | - | 3700<br>610<br>80 | | pF<br>pF<br>pF |
| $C_{oss\ eq.}$ (2) | Equivalent output capacitance | $V_{GS}$=0, $V_{DS}$ =0 to 400 V | - | 325 | | pF |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$= 400 V, $I_D$ = 45 A<br>$V_{GS}$ =10 V<br>*Figure 14* | - | 87<br>23<br>42 | 117 | nC<br>nC<br>nC |
| $R_G$ | Gate input resistance | f=1 MHz Gate DC Bias= 0<br>test signal level = 20 mV<br>open drain | - | 1.7 | | Ω |

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 7. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$ | Turn-on delay time<br>Rise time | $V_{DD}$=250 V, $I_D$= 22.5 A,<br>$R_G$=4.7 Ω, $V_{GS}$=10 V<br>*Figure 15* | - | 26.5<br>107.5 | - | ns<br>ns |
| $t_{r(Voff)}$<br>$t_f$<br>$t_c$ | Off-voltage rise time<br>Fall time<br>Cross-over time | $V_{DD}$=400 V, $I_D$= 45 A,<br>$R_G$=4.7 Ω, $V_{GS}$=10 V<br>*Figure 15* | - | 21.6<br>87.7<br>110.9 | - | ns<br>ns<br>ns |

**Table 8. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 45 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 180 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 45 A, $V_{GS}$ = 0 | - | | 1.5 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$ = 45 A, $V_{DD}$ = 100 V<br>di/dt = 100 A/µs,<br>(see Figure 18) | - | 200<br>1600<br>16 | | ns<br>nC<br>A |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$= 45 A, Tj = 150 °C<br>di/dt = 100 A/µs,<br>$V_{DD}$=100 V, (see Figure 18) | - | 324<br>4017<br>24.8 | | ns<br>nC<br>A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

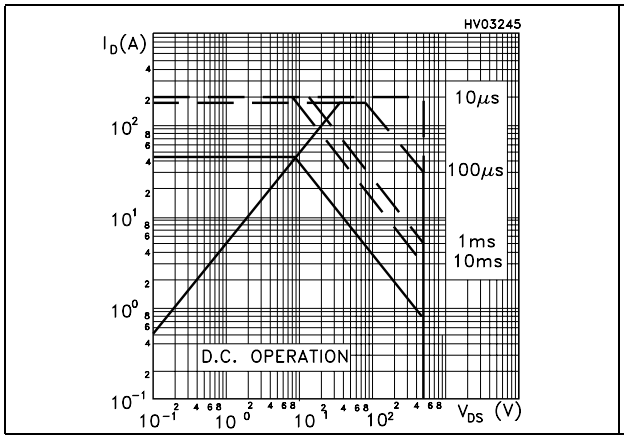



**Figure 3. Thermal impedance**

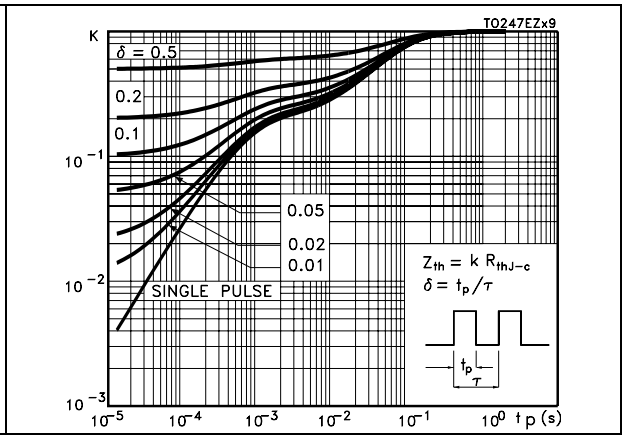



**Figure 4. Output characteristics**

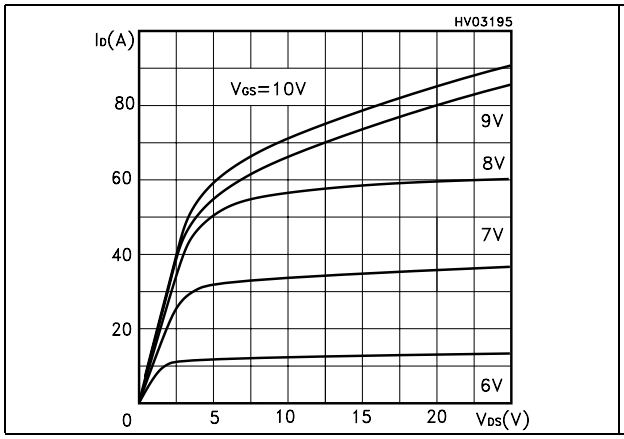



**Figure 5. Transfer characteristics**

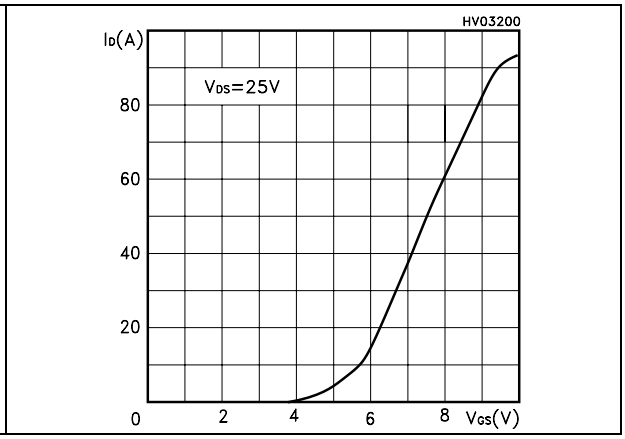



**Figure 6. Transconductance**

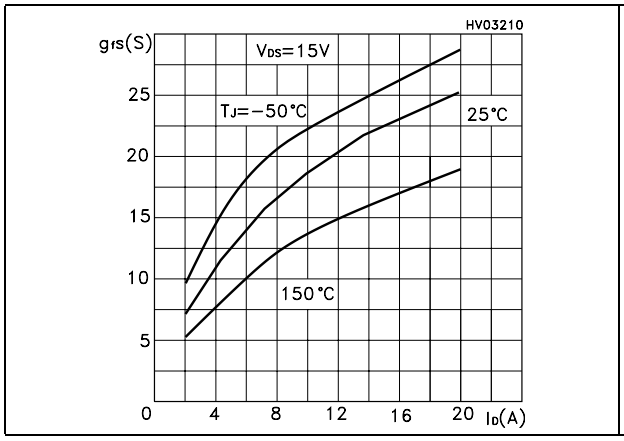



**Figure 7. Static drain-source on resistance**

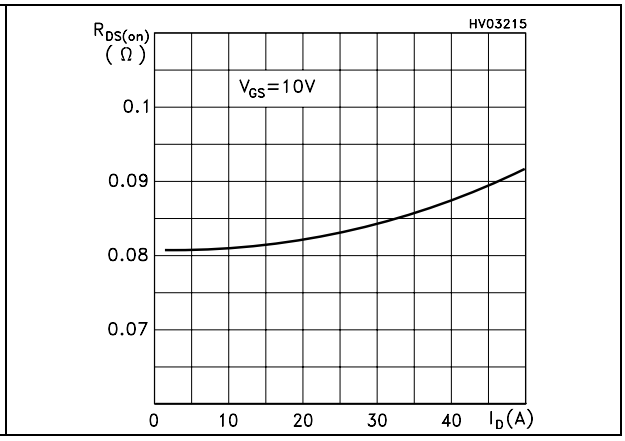


**Figure 8. Gate charge vs gate-source voltage**

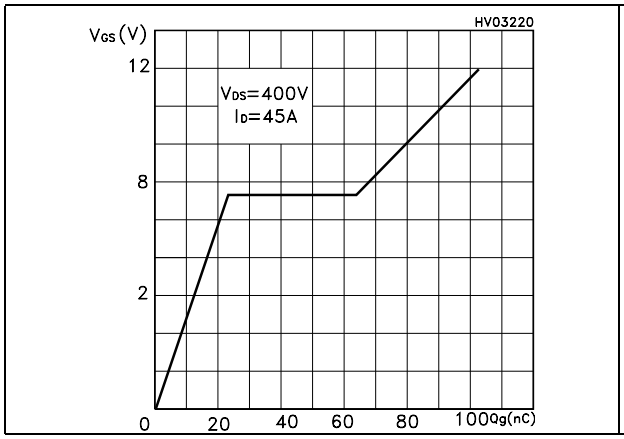



**Figure 9. Capacitance variations**

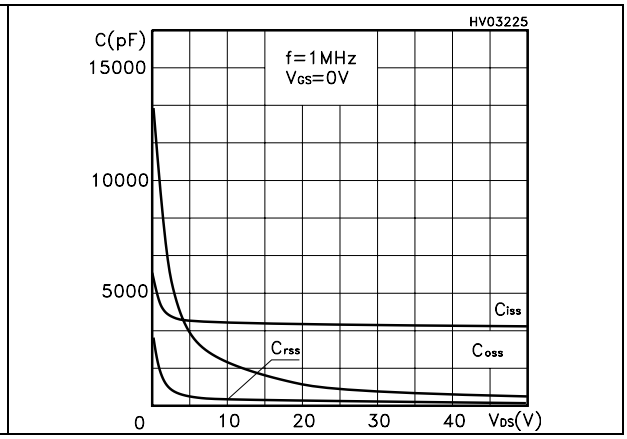



**Figure 10. Normalized gate threshold voltage vs temperature**

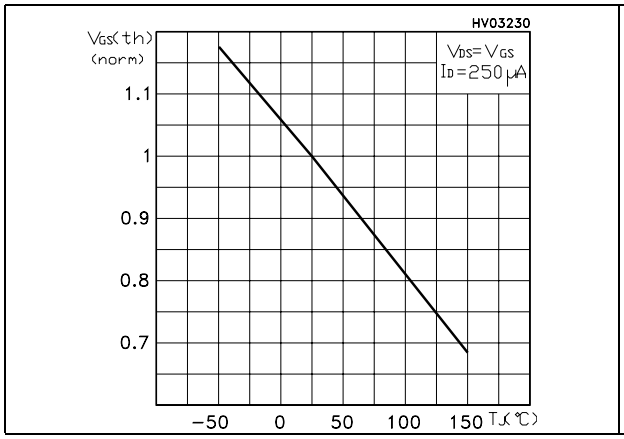



**Figure 11. Normalized on resistance vs temperature**

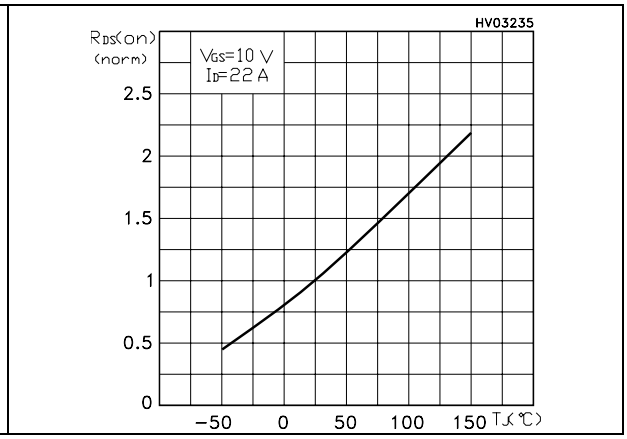
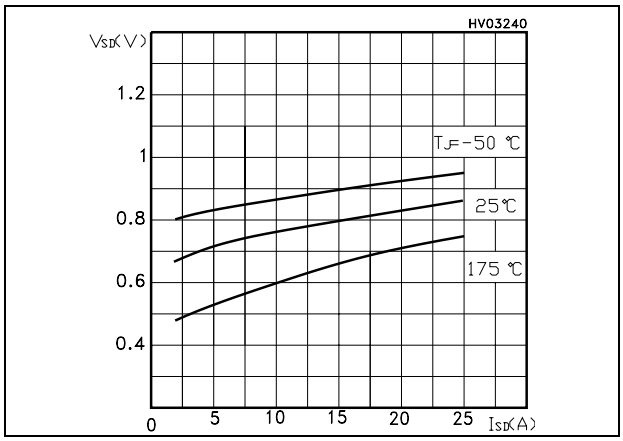



**Figure 12. Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**

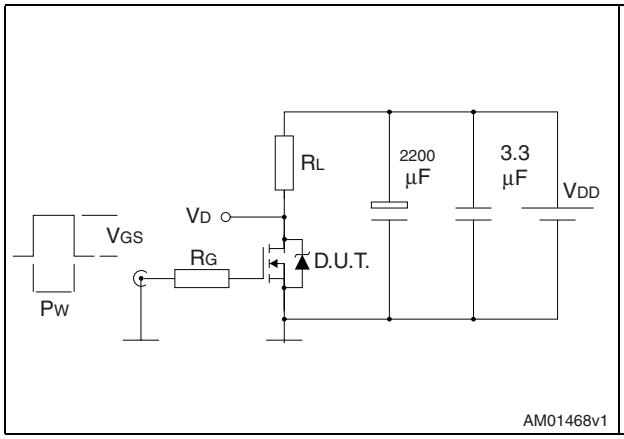



**Figure 14. Gate charge test circuit**

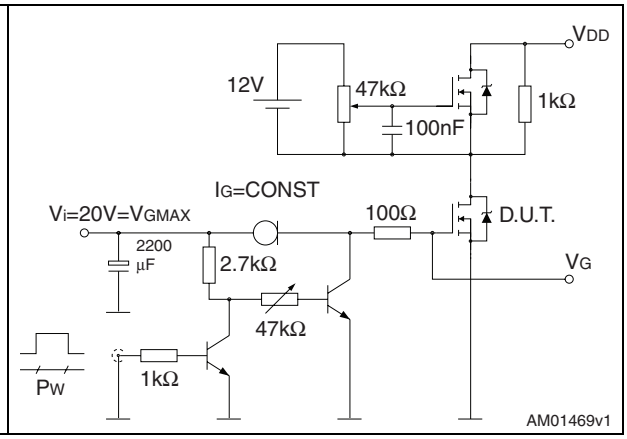



**Figure 15. Test circuit for inductive load switching and diode recovery times**

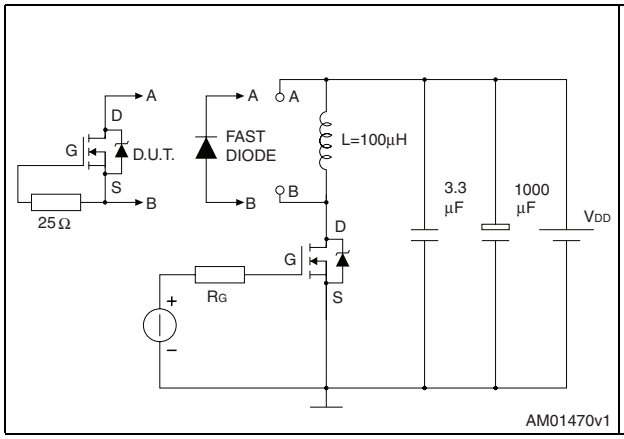



**Figure 16. Unclamped inductive load test circuit**

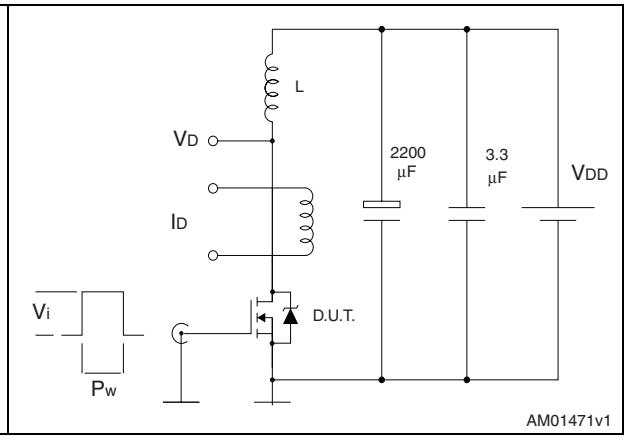



**Figure 17. Unclamped inductive waveform**

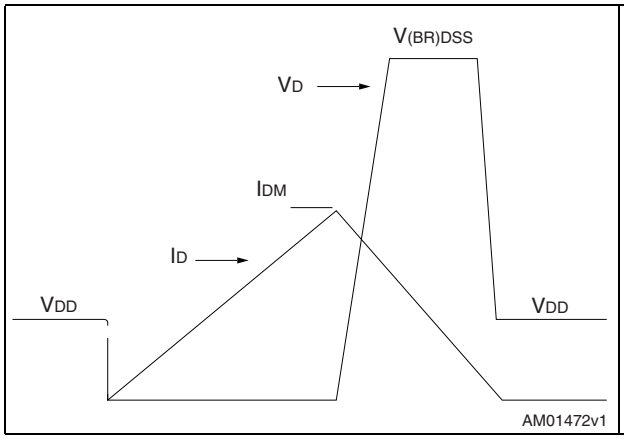
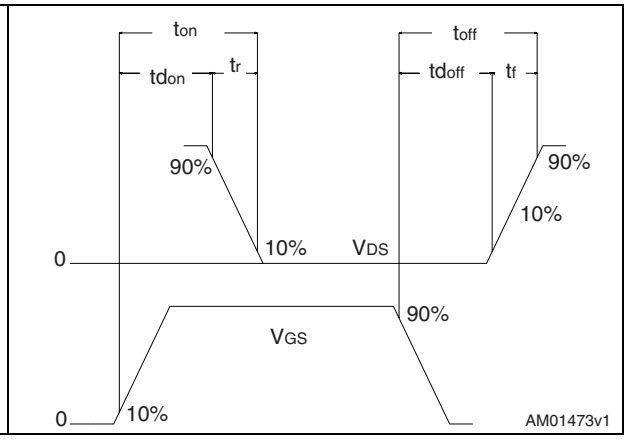



**Figure 18. Switching time waveform**

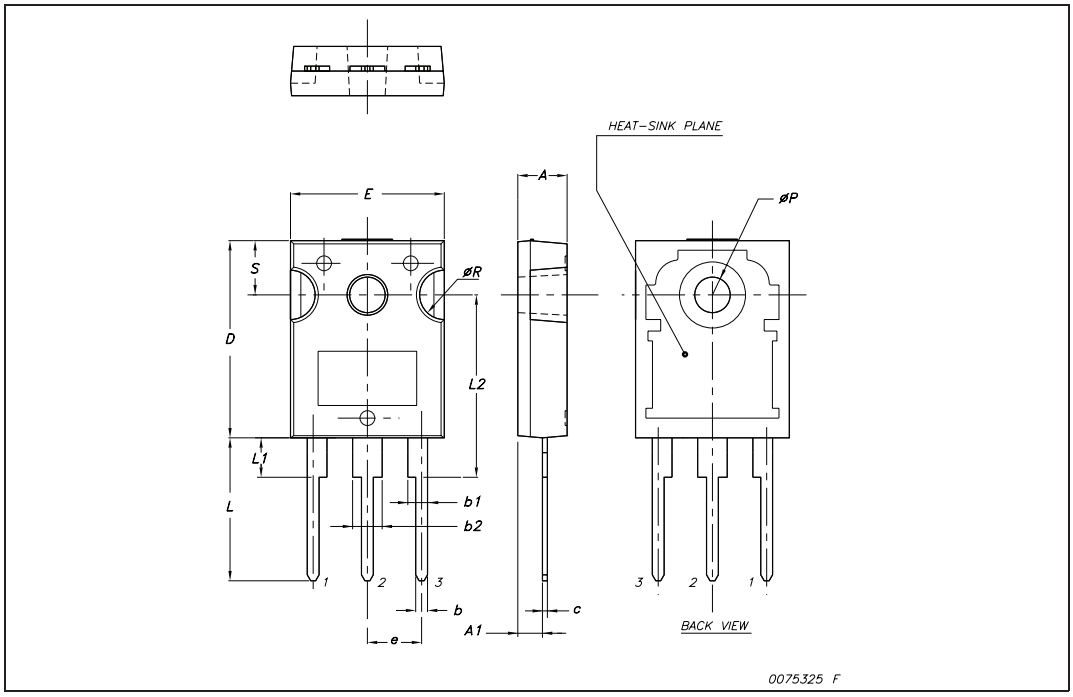


# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

TO-247 Mechanical data

| Dim. | mm. | | |
|---|---|---|---|
| | Min. | Typ | Max. |
| A | 4.85 | | 5.15 |
| A1 | 2.20 | | 2.60 |
| b | 1.0 | | 1.40 |
| b1 | 2.0 | | 2.40 |
| b2 | 3.0 | | 3.40 |
| c | 0.40 | | 0.80 |
| D | 19.85 | | 20.15 |
| E | 15.45 | | 15.75 |
| e | | 5.45 | |
| L | 14.20 | | 14.80 |
| L1 | 3.70 | | 4.30 |
| L2 | | 18.50 | |
| øP | 3.55 | | 3.65 |
| øR | 4.50 | | 5.50 |
| S | | 5.50 | |



# 5 Revision history

**Table 9. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 30-Mar-2005 | 4 | Modified value on *Source drain diode* |
| 23-Jul-2009 | 5 | Modified values on *Switching times* |

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