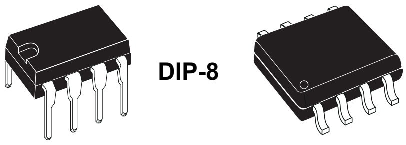
High voltage high and low-side driver

Datasheet - production data



Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability
  - 400 mA source
  - 650 mA sink
- Switching times 50/30 nsec rise/fall with 1 nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis and pull-down
- Internal bootstrap diode
- Outputs in phase with inputs
- Interlocking function

Applications

- Home appliances
- Motor drivers
  - DC, AC, PMDC and PMAC motors
- Lighting applications
- Industrial applications and drives
- Induction heating
- HVAC
- Factory automation
- Power supply systems

Description

The L6387E is a simple and compact high voltage gate driver, manufactured with the BCD™ “offline” technology, and able to drive a half-bridge of power MOS or IGBT devices. The high-side (floating) section is enabled to work with voltage rail up to 600 V. Both device outputs can independently sink and source 650 mA and 400 mA respectively and cannot be simultaneously driven high thanks to an integrated interlocking function.

The L6387E device provides two input pins and two output pins and guarantees the outputs toggle in phase with inputs. The logic inputs are CMOS/TTL compatible to ease the interfacing with controlling devices.

The L6387E features the UVLO protection on the V_{CC} supply voltage and integrates the bootstrap diode, allowing a more compact and reliable solution.

The device is available in a DIP-8 tube and SO-8 tube and tape and reel packaging options.

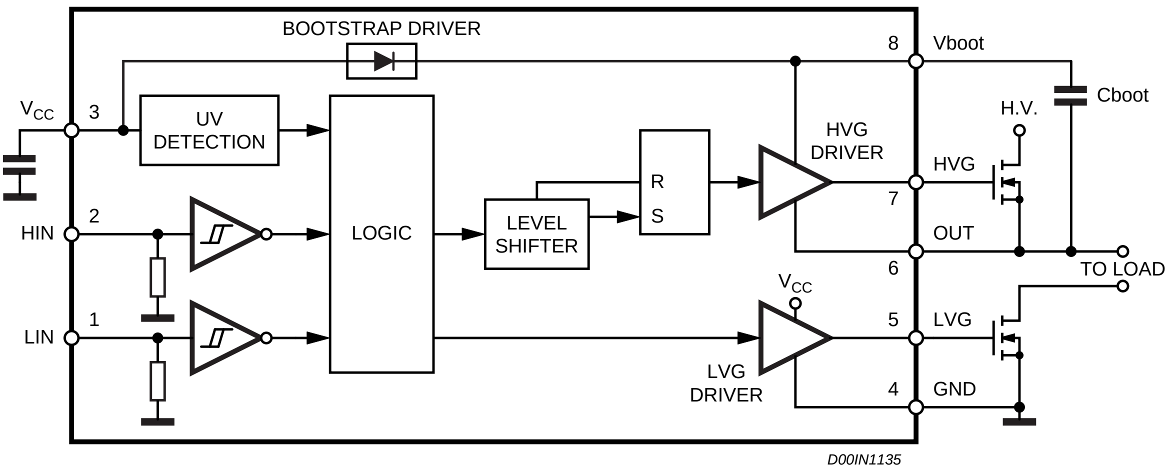
Table 1. Device summary

Part number	Package	Packaging
L6387E	DIP-8	Tube
L6387ED	SO-8	Tube
L6387ED013TR	SO-8	Tape and reel

Contents

1 Block diagram

Figure 1. Block diagram



2 Electrical data

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{out}	Output voltage	-3 to V_{boot} -18	V
V_{cc}	Supply voltage	- 0.3 to +18	V
V_{boot}	Floating supply voltage	-1 to 618	V
V_{hvg}	High-side gate output voltage	-1 to V_{boot}	V
V_{lvg}	Low-side gate output voltage	-0.3 to V_{cc} +0.3	V
V_i	Logic input voltage	-0.3 to V_{cc} +0.3	V
dV_{out}/d_t	Allowed output slew rate	50	V/ns
P_{tot}	Total power dissipation (T_J = 85 °C)	750	mW
T_j	Junction temperature	150	°C
T_s	Storage temperature	-50 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	SO-8	DIP-8	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	150	100	°C/W

2.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{out}	6	Output voltage		(1)		580	V
V_{BS}(2)	8	Floating supply voltage		(1)		17	V
f_{sw}		Switching frequency	HVG, LVG load C_L = 1 nF			400	kHz
V_{cc}	3	Supply voltage				17	V
T_J		Junction temperature		-45		125	°C

1. If the condition V_{boot} - V_{out} < 18 V is guaranteed, V_{out} can range from -3 to 580 V.
2. V_{BS} = V_{boot} - V_{out}.

3 Pin connection

Figure 2. Pin connection (top view)

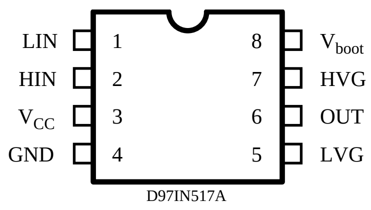


Table 5. Pin description

No.	Pin	Type	Function
1	LIN	I	Low-side driver logic input
2	HIN	I	High-side driver logic input
3	V_{cc}	P	Low voltage power supply
4	GND	P	Ground
5	LVG(1)	O	Low-side driver output
6	OUT	P	High-side driver floating reference
7	HVG(1)	O	High-side driver output
8	V_{boot}	P	Bootstrap supply voltage

1. The circuit guarantees 0.3 V maximum on the pin (at Isink = 10 mA). This allows to omit the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

4 Electrical characteristics

4.1 AC operation

Table 6. AC operation electrical characteristics (V_{CC} = 15 V; T_J = 25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{on}	1 vs. 5 2 vs. 7	High/low-side driver turn-on propagation delay	V_{out} = 0 V		110		ns
t_{off}	1 vs. 5 2 vs. 7	High/low-side driver turn-off propagation delay	V_{out} = 0 V		105		ns
t_r	5, 7	Rise time	C_L = 1000 pF		50		ns
t_f	5, 7	Fall time	C_L = 1000 pF		30		ns

4.2 DC operation

Table 7. DC operation electrical characteristics (V_{CC} = 15 V; T_J = 25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Low supply voltage section							
V_{cc}	3	Supply voltage				17	V
V_{ccth1}		V_{cc} UV turn-on threshold		5.5	6	6.5	V
V_{ccth2}		V_{cc} UV turn-off threshold		5	5.5	6	V
V_{cchys}		V_{cc} UV hysteresis			0.5		V
I_{qccu}		Undervoltage quiescent supply current	$V_{cc} \leq 5$ V		150	220	µA
I_{qcc}		Quiescent current	V_{cc} = 15 V		250	320	µA
R_{dson}		Bootstrap driver on-resistance(1)	$V_{cc} \geq 12.5$ V		125		Ω
Bootstrapped supply voltage section							
V_{BS}	8	Bootstrap supply voltage				17	V
I_{QBS}		V_{BS} quiescent current	HVG ON			100	µA
I_{LK}		High voltage leakage current	$V_{hvg} = V_{out} = V_{boot}$ = 600 V			10	µA
High/low-side driver							
I_{so}	5, 7	Source short-circuit current	$V_{IN} = V_{ih}$ (t_p < 10 µs)	300	400		mA
I_{si}		Sink short-circuit current	$V_{IN} = V_{il}$ (t_p < 10 µs)	450	650		mA

Table 7. DC operation electrical characteristics (continued) (V_{CC} = 15 V; T_J = 25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic inputs							
V_{il}	1, 2	Low level logic threshold voltage				1.5	V
V_{ih}		High level logic threshold voltage		3.6			V
I_{ih}		High level logic input current	V_{IN} = 15 V		50	70	µA
I_{il}		Low level logic input current	V_{IN} = 0 V			1	µA

1. $R_{DS(on)}$ is tested in the following way:

$$R_{DSON} = \frac{(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})}{I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})}$$

where I_1 is the pin 8 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$.

5 Input logic

L6387E input logic is V_{CC} (17 V) compatible. An interlocking feature is offered (see *Table 8*) to avoid undesired simultaneous turn-ON of both power switches driven.

Table 8. Input logic

Input		Output	
HIN	**LIN**	**HVG**	**LVG**
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

6 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (Figure 3 a). In the L6387E device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in Figure 3 b. An internal charge pump (Figure 3 b) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid undesirable turn-on.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value, the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the C_{EXT} and C_{BOOT} capacitors is proportional to the cyclical voltage loss. It has to be:

$$C_{BOOT} >>> C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage losses.

E.g.: HVG steady state consumption is lower than 100 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply a maximum of 0.5 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 0.5 V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has a great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSON} (typical value: 125 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 2

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on-resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

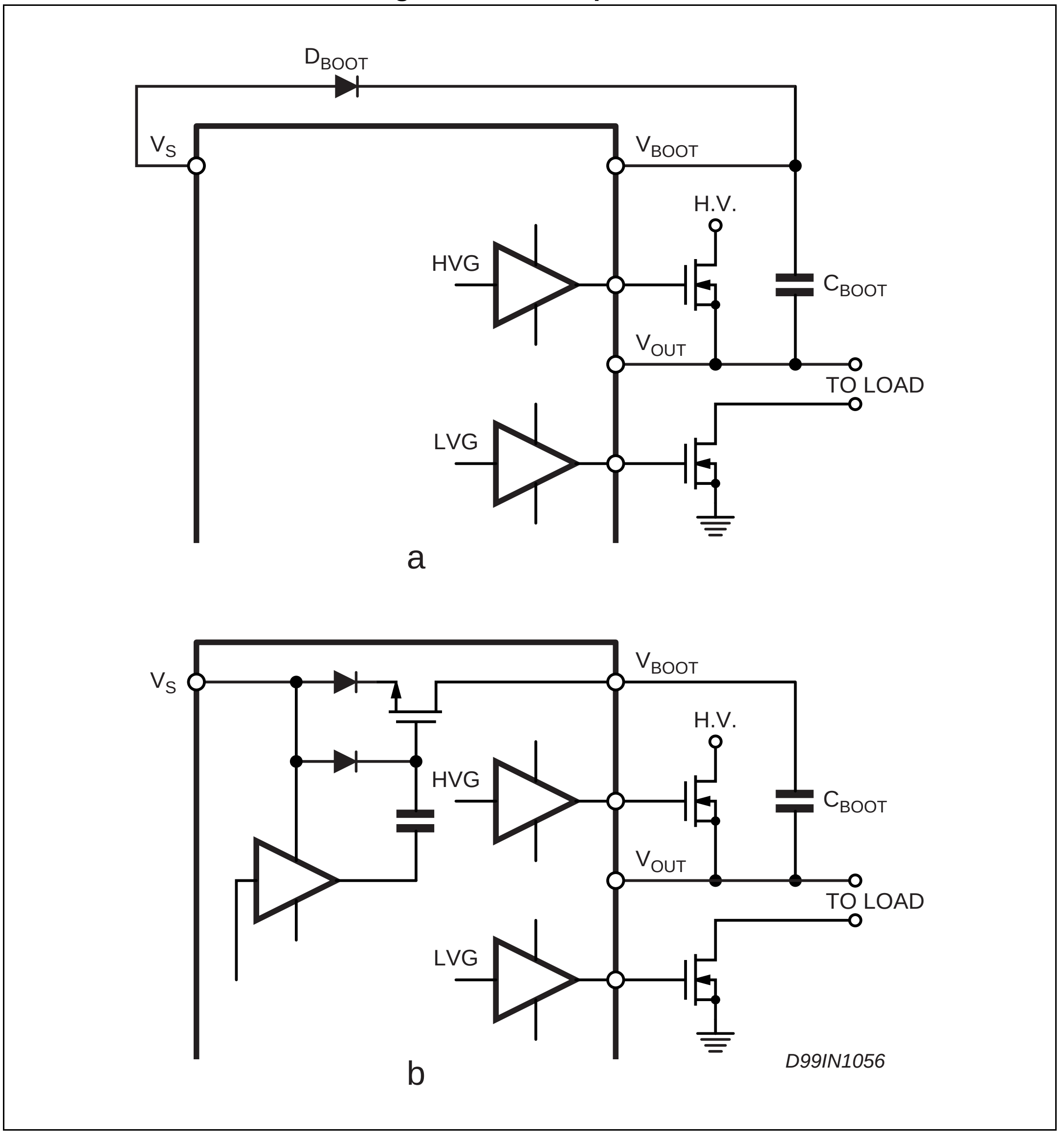
For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5µs. In fact:

Equation 3

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 3. Bootstrap driver



7 Typical characteristic

Figure 4. Typical rise and fall times vs. load capacitance

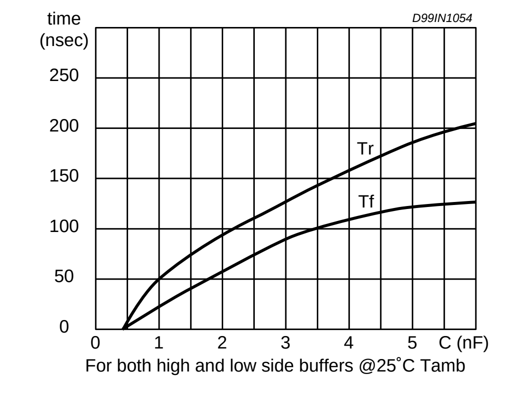


Figure 5. Quiescent current vs. supply voltage

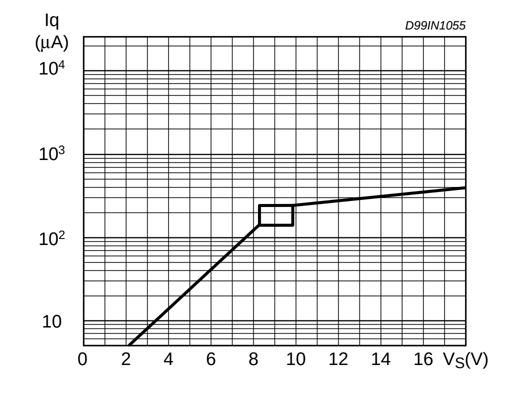


Figure 6. Turn-on time vs. temperature

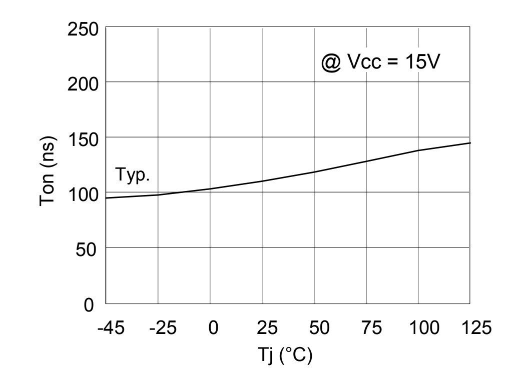


Figure 7. Turn-off time vs. temperature

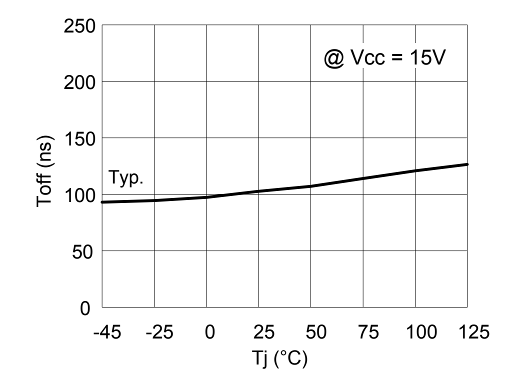


Figure 8. Output source current vs. temperature

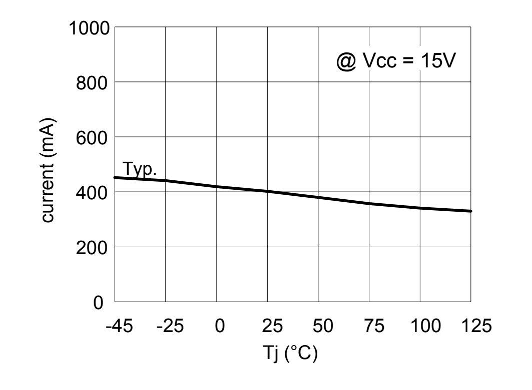
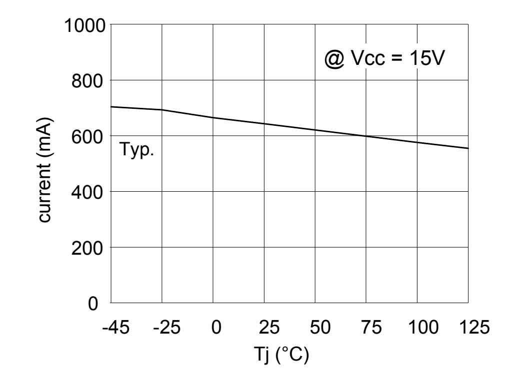


Figure 9. Output sink current vs. temperature



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 10. DIP-8 package outline

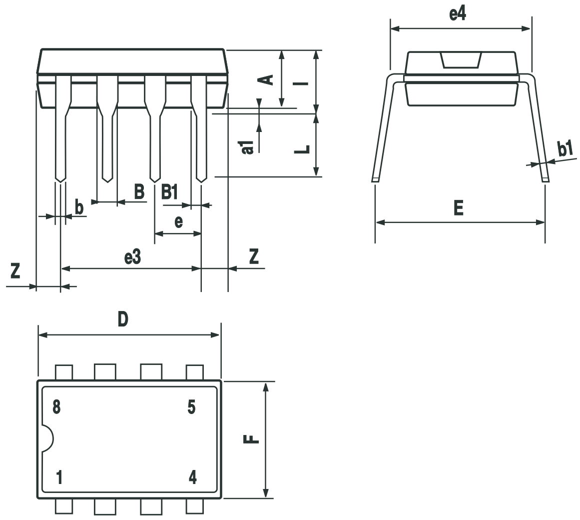


Table 9. DIP-8 package mechanical data

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

Figure 11. SO-8 package outline

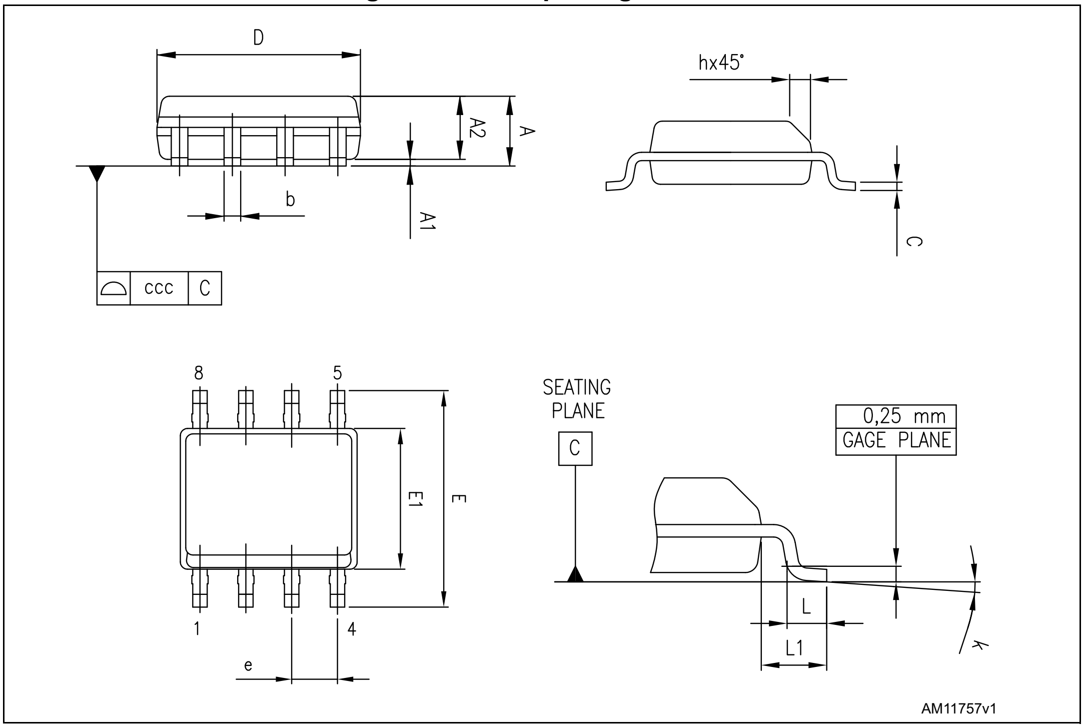


Table 10. SO-8 package mechanical data

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.750			0.0689
A1	0.100		0.250	0.0039		0.0098
A2	1.250			0.0492		
b	0.280		0.480	0.0110		0.0189
c	0.170		0.230	0.0067		0.0091
D(1)	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1(2)	3.800	3.900	4.000	0.1496	0.1535	0.1575
e		1.270			0.0500	
h	0.250		0.500	0.0098		0.0197
L	0.400		1.270	0.0157		0.0500
L1		1.040			0.0409	
k	0°		8°	0°		8°
ccc			0.10			0.0039

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both sides).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

9 Revision history

Table 11. Document revision history

Date	Revision	Changes
11-Oct-2007	1	First release
19-Sep-2008	2	Minor text changes on *Table 7*
19-Jun-2014	3	Added *Section : Applications on page 1*. Updated *Section : Description on page 1* (replaced by new description). Updated *Table 1: Device summary on page 1* (moved from page 15, updated title). Updated *Figure 1: Block diagram on page 3* (moved from page 1 to page 3, added title to *Section 1: Block diagram on page 3*). Updated *Section 2.1: Absolute maximum ratings on page 4* (removed note below *Table 2: Absolute maximum ratings*). Updated *Table 5: Pin description on page 5* (updated “Pin” and “Types”). Added cross-references in *Section 5: Input logic on page 8*. Updated *Section 6: Bootstrap driver on page 9* (updated values of “E.g.: HVG”). Numbered *Equation 1 on page 9*, *Equation 2 on page 9* and *Equation 3 on page 10*. Updated *Section 8: Package information on page 12* [updated/added titles, reversed order of *Figure 10* and *Table 9*, *Figure 11* and *Table 10* (numbered tables), removed 3D package figures, minor modifications]. Minor modifications throughout document.