DPA422-426

DPA-Switch® Family

Highly Integrated DC-DC Converter ICs for Power over Ethernet & Telecom Applications

Product Highlights

Highly Integrated Solution

- Eliminates up to 50 external components–saves space, cost
- Integrates 220 V high frequency MOSFET, PWM control
- Lower cost plastic DIP surface mount (G package) and through-hole (P package) options for designs ≤35 W
- Thermally efficient MO-169-7C (S-PAK) and TO-263-7C (R package) options for high power applications

Superior Performance and Flexibility

- Eliminates all external current sensing circuitry
- Built-in auto-restart for output overload/open loop protection
- Pin selectable 300/400 kHz fixed frequency
- Wide input (line) voltage range: 16-75 VDC
- Externally programmable current limit
- Source connected tab reduces EMI
- Line under-voltage (UV) detection: meets ETSI standards
- Line overvoltage (OV) shutdown protection
- UV/OV limits gate drive voltage for synchronous rectification
- Fully integrated soft-start for minimum stress/overshoot
- Supports forward or flyback topology
- Cycle skipping: regulation to zero load without pre-load
- Hysteretic thermal shutdown for automatic fault recovery
- RoHS compliant P, G and S package options

EcoSmart®– Energy Efficient

- Extremely low consumption at no load
- Cycle skipping at light load for high standby efficiency

Applications

- PoE applications, VoIP phones, WLAN, security cameras
- Telco central office equipment: xDSL, ISDN, PABX
- Distributed power architectures (24 V/48 V bus)
- Industrial controls

Description

The *DPA-Switch* IC family is a highly integrated solution for DC-DC conversion applications with 16-75 VDC input.

DPA-Switch uses the same proven topology as *TOPSwitch*®, cost effectively integrating a power MOSFET, PWM control, fault protection and other control circuitry onto a single CMOS chip. High performance features are enabled with three user configurable pins. Hysteretic thermal shutdown is also provided. In addition, all critical parameters (i.e. current limit, frequency, PWM gain) have tight temperature and absolute tolerance, to simplify design and reduce system cost.

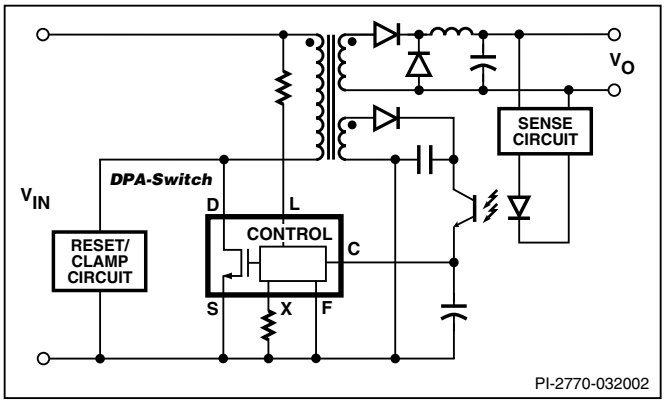

Figure 1. Typical Forward Converter Application.

OUTPUT POWER TABLE						
36-75 VDC INPUT RANGE (FORWARD)[2]						
Total Device Dissipation[3] / PRODUCT[4]	**0.5 W**	**1 W**	**2.5 W**	**4 W**	**6 W**	**Max Power Output[1]**
DPA422[7]	7.5 W	10 W	-	-	-	10 W
DPA423	12 W	16 W	-	-	-	18 W
DPA424	16 W	23 W	35 W	-	-	35 W
DPA425	23 W	32 W	50 W	62 W	-	70 W
DPA426[5]	25 W	35 W	55 W	70 W	83 W	100 W
36-75 VDC INPUT RANGE (FLYBACK)[2]						
Total Device Dissipation[3] / PRODUCT[4]	**0.5 W**	**0.75 W**	**1 W**	**1.5 W**		**Max Power Output[1]**
DPA422	6.5 W	9.0 W	-	-		9.0 W
DPA423	9 W	13 W	-	-		13 W
DPA424	10 W	14.5 W	18 W	24 W		26 W
DPA425	-[6]	-[6]	-[6]	25.5 W		52 W

Table 1.Output Power Table. Notes:**1.** Maximum output power is limited by device internal current limit. **2.** See Applications Considerations section for complete description of assumptions and for output powers with other input voltage ranges. **3.** For device dissipation of 1.5 W or below, use P or G packages. Device dissipation above 1.5 W is possible with S and R packages. **4.** Packages: P: DIP-8, G: SMD-8, R: TO-263-7C, S: MO-169-7C. For lead-free package options, see Part Ordering Information. **5.** Available in S and R package only. **6.** Due to higher switching losses, the DPA425 may not deliver additional power compared to a smaller device. **7.** Available in P and G package only.

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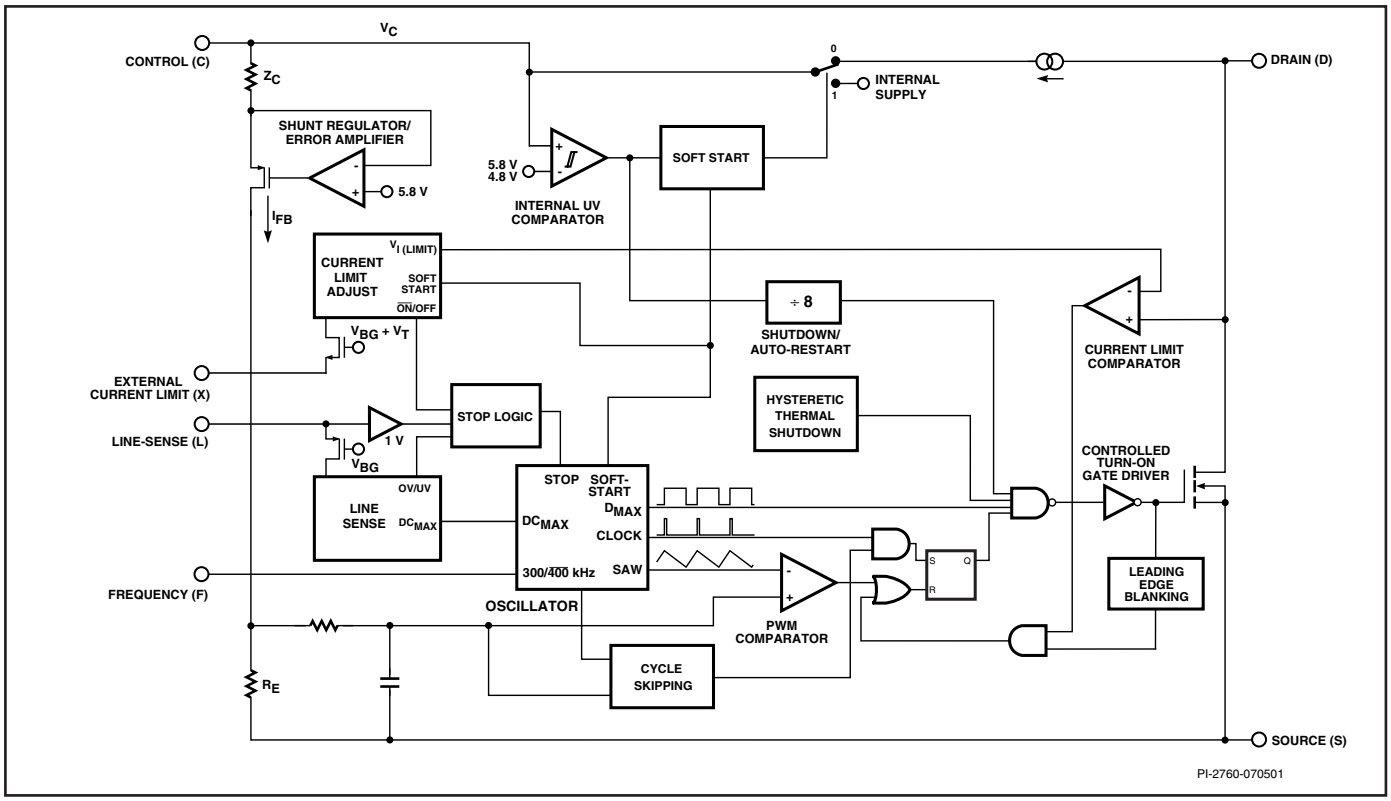


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
High voltage power MOSFET drain output. The internal startup bias current is

Figure 3. Pin Configuration (Top View).

DPA-Switch Family Functional Description

DPA-Switch is an integrated switched mode power supply chip that converts a current at the control input to a duty cycle at the open drain output of a high voltage power MOSFET. During normal operation the duty cycle of the power MOSFET decreases linearly with increasing CONTROL pin current as shown in Figure 4. A patented high-voltage CMOS technology allows both the high-voltage power MOSFET and all the low voltage control circuitry to be cost effectively integrated onto a single monolithic chip.

In addition to the standard *TOPSwitch* features, such as the high-voltage start-up, the cycle-by-cycle current limiting, loop compensation circuitry, auto-restart and thermal shutdown, *DPA-Switch* also offers many advanced features that reduce system cost and increase power supply performance and design flexibility. Following is a summary of the advanced features:

1. A fully integrated 5 ms soft-start limits peak currents and voltages during start-up and reduces or eliminates output overshoot in most applications.
2. A 75% maximum duty cycle (DC_{MAX}) together with the line feed-forward with DC_{MAX} reduction feature makes *DPA-Switch* well suited for both flyback and forward topologies.
3. High switching frequency (400 kHz/300 kHz, pin selectable) allows the use of smaller size transformers and offers high bandwidth for power supply control loop.
4. Cycle skipping operation at light load minimizes standby power consumption (typically <10 mA input current).
5. Line under-voltage ensures glitch free operations at both power-up and power-down and is tightly toleranced over process and temperature to meet system level requirements common in DC to DC converters (e.g. ETSI).
6. Line overvoltage protects *DPA-Switch* against excessive input voltage and line surge.
7. External current limit adjustment allows the setting of the current limit externally to a lower level near the operating peak current and, if desired, further adjusts the level gradually as line voltage rises. This makes possible an ideal implementation of overload power limiting.
8. Synchronization function allows the synchronization of *DPA-Switch* operation to an external lower frequency.
9. Remote ON/OFF feature permits *DPA-Switch* based power supplies to be easily switched on/off using logic signals. Maximum input current consumption is 2 mA in remote OFF.
10. Hysteretic over-temperature shutdown provides automatic recovery from thermal fault.
11. Tight absolute tolerances and small temperature variations on switching frequency, current limit, and under-voltage lock out threshold (UV).

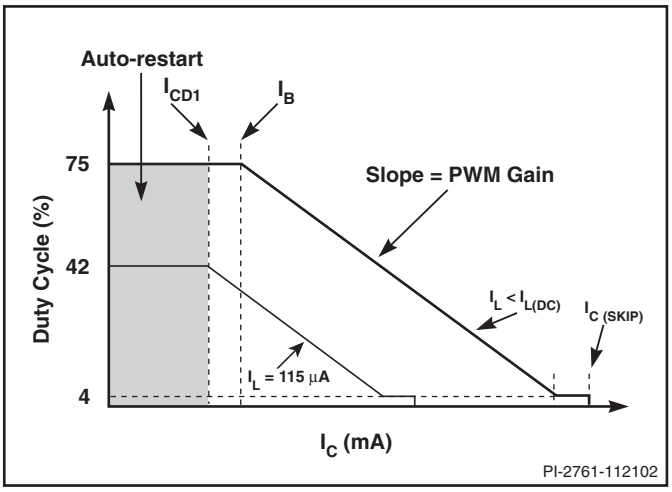


Figure 4. Relationship of Duty Cycle to CONTROL Pin Current.

Three pins, LINE-SENSE (L), EXTERNAL CURRENT LIMIT (X) and FREQUENCY (F), are used to implement all the pin - controllable features. A resistor from the LINE-SENSE pin to DC input bus implements line UV, line OV and line feed-forward with DC_{MAX} reduction. A resistor from the EXTERNAL CURRENT LIMIT pin to the SOURCE pin sets current limit externally. In addition, remote ON/OFF may be implemented through either the LINE-SENSE pin or the EXTERNAL CURRENT LIMIT pin depending on the polarity of the logic signal available as well as other system specific considerations. Shorting both the LINE-SENSE and the EXTERNAL CURRENT LIMIT pins to the SOURCE pin disables line OV, line UV, line feed-forward with DC_{MAX} reduction, external current limit, remote ON/OFF and synchronization. The FREQUENCY pin sets the switching frequency to 400 kHz if connected to the SOURCE pin, or 300 kHz if connected to the CONTROL pin. This pin should not be left open. Please refer to "Using Feature Pins" section for detailed information regarding the proper use of those pins.

CONTROL (C) Pin Operation

The CONTROL pin is a low impedance node that is capable of receiving a combined supply and feedback current. During normal operation, a shunt regulator is used to separate the feedback signal from the supply current. CONTROL pin voltage V_C is the supply voltage for the control circuitry including the MOSFET gate driver. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the instantaneous gate drive current. The total amount of capacitance connected to this pin also sets the auto-restart timing as well as control loop compensation.

When the DC input voltage is applied to the DRAIN pin during start-up, the MOSFET is initially off, and the CONTROL pin capacitor is charged through the switched high voltage current source connected internally between the DRAIN and CONTROL pins. When the CONTROL pin voltage V_C reaches

approximately 5.8 V, the control circuitry is activated and the soft-start begins. The soft-start circuit gradually increases the duty cycle of the MOSFET from zero to the maximum value over approximately 5 ms. The high voltage current source is turned off at the end of the soft-start. If no external feedback/supply current is fed into the CONTROL pin by the end of the soft-start, the CONTROL pin will start discharging in response to the supply current drawn by the control circuitry and the gate current of the switching MOSFET driver. If the power supply is designed properly, and no fault condition such as open loop or overloaded output exists, the feedback loop will close, providing external CONTROL pin current, before the CONTROL pin voltage has had a chance to discharge to the lower threshold voltage of approximately 4.8 V (internal supply under-voltage lockout threshold). When the externally fed current charges the CONTROL pin to the shunt regulator voltage of 5.8 V, current in excess of the consumption of the chip is shunted to SOURCE through resistor R_E as shown in Figure 2. This current flowing through R_E controls the duty cycle of the power MOSFET to provide closed loop regulation. The shunt regulator has a finite low output impedance Z_C that sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance Z_C of the CONTROL pin together with the external CONTROL pin capacitance sets the dominant pole for the control loop.

When a fault condition such as an open loop or overloaded output prevents the flow of an external current into the CONTROL pin, the capacitor on the CONTROL pin discharges towards 4.8 V. At 4.8 V auto-restart is activated which turns the output MOSFET off and puts the control circuitry in a low current standby mode. The high-voltage current source turns on and charges the external capacitance again. A hysteretic internal supply under-voltage comparator keeps V_C within a window of typically 4.8 V to 5.8 V by turning the high-voltage current source on and off as shown in Figure 5. The auto-restart circuit has a divide-by-8 counter that prevents the output MOSFET from turning on again until eight discharge/charge cycles have elapsed. This is accomplished by enabling the output MOSFET only when the divide-by-8 counter reaches full count (S7). The counter effectively limits *DPA-Switch* power dissipation as well as the maximum power delivered to the power supply output by reducing the auto-restart duty cycle to typically 4%. Auto-restart mode continues until output voltage regulation is again achieved through closure of the feedback loop.

Oscillator and Switching Frequency

The internal oscillator linearly charges and discharges an internal capacitance between two voltage levels to create a sawtooth waveform for the pulse width modulator. The oscillator sets both the pulse width modulator latch and the current limit latch at the beginning of each cycle.

The nominal switching frequency of 400 kHz was chosen to minimize the transformer size and to allow faster power supply loop response. The FREQUENCY pin, when shorted to the CONTROL pin, lowers the switching frequency to 300 kHz, which may be preferable in some applications such as those employing secondary synchronous rectification. Otherwise, the FREQUENCY pin should be connected to the SOURCE pin for the default 400 kHz.

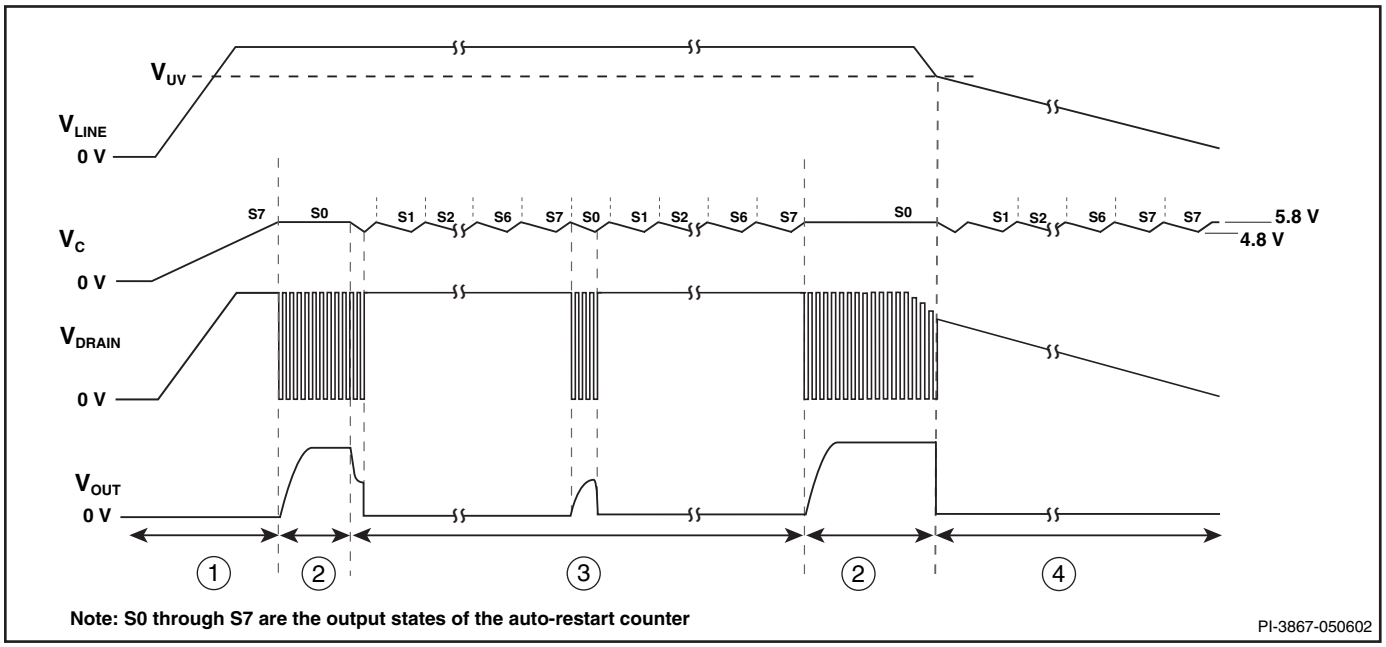


Figure 5. Typical Waveforms for (1) Power Up, (2) Normal Operation; (3) Auto-restart and (4) Power Down.

Pulse Width Modulator and Maximum Duty Cycle
The pulse width modulator implements voltage mode control by driving the output MOSFET with a duty cycle inversely proportional to the current into the CONTROL pin that is in excess of the internal supply current of the chip (see Figure 4). The excess current is the feedback error signal that appears across R_E (see Figure 2). This signal is filtered by an RC network with a typical corner frequency of 30 kHz to reduce the effect of switching noise in the chip supply current generated by the MOSFET gate driver. The filtered error signal is compared with the internal oscillator sawtooth waveform to generate the duty cycle waveform. As the control current increases, the duty cycle decreases. A clock signal from the oscillator sets a latch that turns on the output MOSFET. The pulse width modulator resets the latch, turning off the output MOSFET. Note that a minimum current must be driven into the CONTROL pin before the duty cycle begins to change.

The maximum duty cycle, DC_{MAX} is set at a default maximum value of 75% (typical). However, by connecting the LINE-SENSE to the DC input bus through a resistor with appropriate value, the maximum duty cycle can be made to decrease from 75% to 33% (typical) as shown in Figure 7 when input line voltage increases (see Line Feed-Forward with DC_{MAX} Reduction).

Minimum Duty Cycle and Cycle Skipping
To maintain power supply output regulation, the pulse width modulator reduces duty cycle as the load at the power supply output decreases. This reduction in duty cycle is proportional to the current flowing into the CONTROL pin. As the CONTROL pin current increases, the duty cycle reduces linearly towards a minimum value specified as minimum duty cycle, DC_{MIN}. After reaching DC_{MIN}, if CONTROL pin current is increased further by approximately 2 mA, the pulse width modulator will force the duty cycle from DC_{MIN} to zero in a discrete step (refer to Figure 4). This feature allows a power supply to operate in a cycle skipping mode when the load consumes less power than the *DPA-Switch* delivers at minimum duty cycle, DC_{MIN}. No additional control is needed for the transition between normal operation and cycle skipping. As the load increases or decreases, the power supply automatically switches between normal and cycle skipping mode as necessary.

Cycle skipping may be avoided, if so desired, by connecting a minimum load at the power supply output such that the duty cycle remains at a level higher than DC_{MIN} at all times.

Error Amplifier
The shunt regulator can also perform the function of an error amplifier in primary side feedback applications. The shunt regulator voltage is accurately derived from a temperature-compensated bandgap reference. The gain of the error amplifier is set by the CONTROL pin dynamic impedance. The CONTROL pin clamps external circuit signals to the V_C voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and flows through R_E as a voltage error signal.

On-chip Current Limit with External Programmability
The cycle-by-cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET on-state drain to source voltage, $V_{DS(ON)}$ with a threshold voltage. At the current limit, $V_{DS(ON)}$ exceeds the threshold voltage and the MOSFET is turned off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature compensated to minimize the variation of the current limit due to temperature related changes in $R_{DS(ON)}$ of the output MOSFET. The default current limit of *DPA-Switch* is preset internally. However, with a resistor connected between EXTERNAL CURRENT LIMIT pin and SOURCE pin, the current limit can be programmed externally to a lower level between 25% and 100% of the default current limit. Please refer to the graphs in the Typical Performance Characteristics section for the selection of the resistor value. By setting current limit low, a larger *DPA-Switch* than necessary for the power required can be used to take advantage of the lower $R_{DS(ON)}$ for higher efficiency/smaller heat sinking requirements. With a second resistor connected between the EXTERNAL CURRENT LIMIT pin and the DC input bus, the current limit is reduced with increasing line voltage, allowing a true power limiting operation against line variation to be implemented in a flyback configuration.

The leading edge blanking circuit inhibits the current limit comparator for a short time after the output MOSFET is turned on. The leading edge blanking time has been set so that, if a power supply is designed properly, current spikes caused by primary-side capacitance and secondary-side rectifier reverse recovery time should not cause premature termination of the switching pulse.

The current limit after the leading edge blanking time is as shown in Figure 31. To avoid triggering the current limit in normal operation, the drain current waveform should stay within the envelope shown.

Line Under-Voltage Detection (UV)
At power up**,** UV keeps *DPA-Switch* off until the input line voltage reaches the under voltage upper threshold. At power down, UV holds *DPA-Switch* on until the input voltage falls below the under voltage lower threshold. A single resistor connected from the LINE-SENSE pin to the DC input bus sets UV upper and lower thresholds. To avoid false triggering by noise, a hysteresis is implemented which sets the UV lower threshold typically at 94% of the UV upper threshold. If the UV lower threshold is reached during operation without the power supply losing regulation and the condition stays longer than 10 µs (typical), the device will turn off and stay off until the

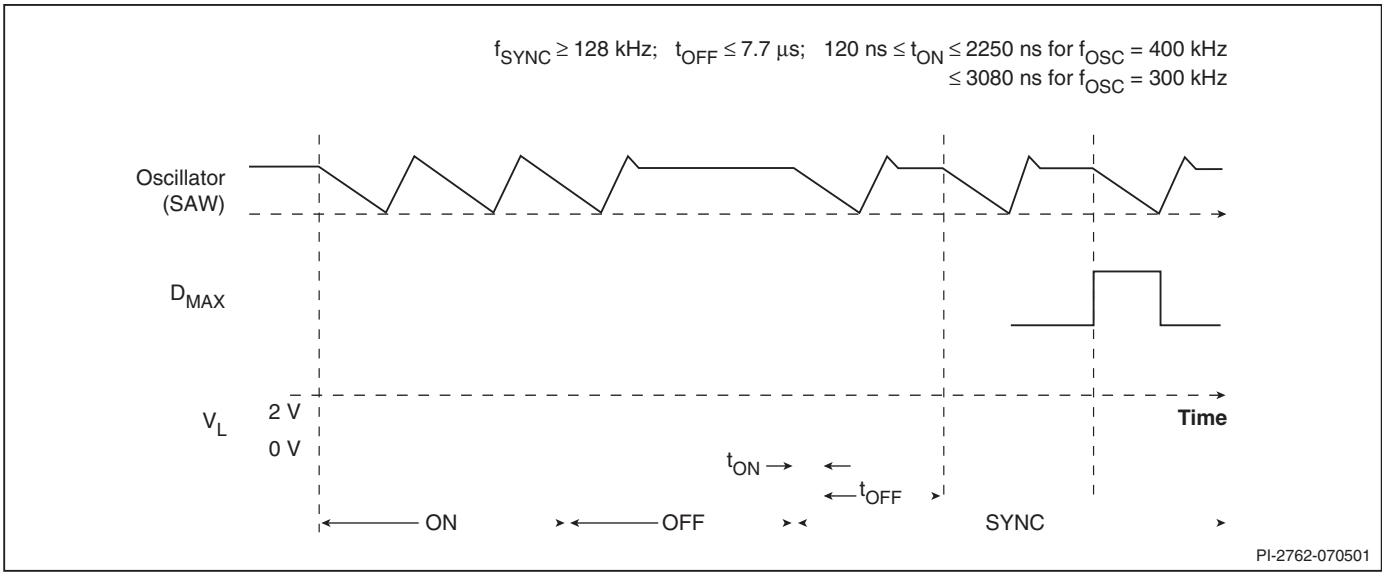


Figure 6. Synchronization Timing Diagram.

(typical), the CONTROL pin goes into the hysteretic mode of operation. In this mode, the CONTROL pin goes through alternate charge and discharge cycles between 4.8 V and 5.8 V (see CONTROL Pin Operation section above) and the IC runs entirely off the high voltage DC input, but with very low power consumption (30 mW typical at 48 V with LINE-SENSE and EXTERNAL CURRENT LIMIT pins open). When the *DPA-Switch* is remotely turned on after entering this mode, it will initiate a normal start-up sequence with soft-start the next time the CONTROL pin reaches 5.8 V. In the worst case, the delay from remote on to start-up can be equal to the full discharge/charge cycle time of the CONTROL pin, which is approximately 36 ms for a 22 µF CONTROL pin capacitor. This reduced-consumption remote-off mode can eliminate expensive and unreliable in-line mechanical switches. It also allows for microprocessor-controlled turn-on and turn-off sequences that may be required in certain applications.

Synchronization

In addition to sensing incoming current for OV, UV and remote ON/OFF, the LINE-SENSE pin also monitors its pin voltage through a 1 V threshold comparator. A pin voltage below 1 V turns on *DPA-Switch*. When the voltage at LINE-SENSE pin rises beyond 1 V to disable the output, *DPA-Switch* completes its current switching cycle before the output is forced off (similar to remote ON/OFF operation). The internal oscillator is stopped at the end of the current cycle awaiting the LINE-SENSE pin voltage to go low to start the next cycle. This allows the use of the 1 V threshold to synchronize *DPA-Switch* to an external signal with a frequency lower than its internal switching frequency. A transistor or an optocoupler output connected between the LINE-SENSE pin and the SOURCE pin implements this function (see Figure 24). Please refer to Figure 6 for the timing waveforms of synchronization operation.

In order to be recognized as a synchronization pulse, the LINE-SENSE pin needs to stay low (on-time) for at least 120 ns but no more than 2250 ns for 400 kHz (or 3080 ns for 300 kHz) internal switching frequency. In addition, the off-time must be kept below 7.7 µs, which is a limitation set by the lowest synchronization frequency of 128 kHz allowed by the chip. The effective DC_{MAX} for synchronization operation can be calculated as $0.75 \cdot f_{SYNC}/f_{OSC}$. An off-time longer than 7.7 µs may force the CONTROL pin to go into the hysteretic mode and initiate a soft-start cycle at next turn-on.

Soft-Start

Two on-chip soft-start functions are activated at start-up with a duration of 5 ms (typical). Maximum duty cycle starts from 0% and linearly increases to the default maximum of 75% at the end of the 5 ms duration and the current limit starts from about 85% and linearly increases to 100% at the end of the 5 ms duration. In addition to start-up, soft-start is also activated at each restart attempt during auto-restart and when restarting after being in hysteretic regulation of CONTROL pin voltage (V_C), due to remote off or thermal shutdown conditions. This effectively minimizes current and voltage stresses on the output MOSFET, the clamp circuit and the output rectifier during start-up. This feature also helps minimize output overshoot and prevents saturation of the transformer during start-up.

Shutdown/Auto-Restart

To minimize *DPA-Switch* power dissipation under fault conditions, the shutdown/auto-restart circuit turns the power supply on and off at an auto-restart duty cycle of typically 4% if an out of regulation condition persists. Loss of regulation interrupts the external current into the CONTROL pin. V_C regulation changes from shunt mode to the hysteretic auto-restart mode as described in CONTROL pin operation section. When the fault condition is removed, the power supply output becomes regulated, V_C regulation returns to shunt mode, and normal operation of the power supply resumes.

Hysteretic Over-Temperature Protection

Over temperature protection is provided by a precision analog circuit that turns the output MOSFET off when the junction temperature exceeds the thermal shutdown temperature (137 °C typical). When the junction temperature cools to below the hysteretic temperature (110 °C typical), normal operation resumes providing automatic recovery. V_C is regulated in hysteretic mode and a 4.8 V to 5.8 V (typical) sawtooth waveform is present on the CONTROL pin while in thermal shutdown.

Bandgap Reference

All critical *DPA-Switch* internal voltages are derived from a temperature-compensated bandgap reference. This reference is also used to generate a temperature-compensated current reference that is trimmed to accurately set the switching frequency, current limit, and the line OV/UV thresholds. *DPA-Switch* has improved circuitry to maintain all of the above critical parameters within very tight absolute and temperature tolerances.

High-Voltage Bias Current Source

This current source biases *DPA-Switch* from the DRAIN pin and charges the CONTROL pin external capacitance during start-up or hysteretic operation. Hysteretic operation occurs during auto-restart, remote off and over-temperature shutdown. In this mode of operation, the current source is switched on and off with an effective duty cycle of approximately 20%. This duty cycle is determined by the ratio of CONTROL pin charge ($I_{C(CH)}$) and discharge currents (I_{CD1} and I_{CD2}). This current source is turned off during normal operation when the output MOSFET is switching. The effect of the current source switching may be seen on the DRAIN voltage waveform as small disturbances, which is normal.

Using Feature Pins

FREQUENCY (F) Pin Operation

The FREQUENCY pin is a digital input pin. Shorting the FREQUENCY pin to SOURCE pin selects the nominal switching frequency of 400 kHz (Figure 9) which is suited for most applications. For other applications that may benefit from lower switching frequency, a 300 kHz switching frequency can be selected by shorting the FREQUENCY pin to the CONTROL pin (Figure 10). This pin should not be left open.

LINE-SENSE (L) Pin Operation

When current is fed into the LINE-SENSE pin, it works as a voltage source of approximately 2.6 V up to a maximum current of +240 µA (typical). At +240 µA, this pin turns into a constant current sink. Refer to Figure 8. In addition, a comparator with a threshold of 1 V is connected at the pin and is used to detect when the pin is shorted to the SOURCE pin.

There are a total of five functions available through the use of the LINE-SENSE pin: OV, UV, line feed-forward with DC_{MAX} reduction, remote ON/OFF and synchronization. Shorting the LINE-SENSE pin to the SOURCE pin disables all five functions. The LINE-SENSE pin is typically used for line sensing by connecting a resistor from this pin to the positive input DC voltage bus to implement OV, UV and line feed-forward with DC_{MAX} reduction over line voltage. In this mode, the value of the resistor determines the line OV/UV thresholds, and the DC_{MAX} is reduced linearly with input DC high voltage starting from just above the UV threshold. This pin can also be used as the input pin for remote ON/OFF and synchronization. An external transistor placed between the LINE-SENSE pin and the CONTROL pin realizes remote ON/OFF via UV or OV threshold. Synchronization is available by connecting an open drain external MOSFET between the LINE-SENSE pin and the SOURCE pin to generate synchronization pulse. Each time the MOSFET turns on, the falling edge of the LINE-SENSE pin voltage initiates a new switching cycle. The lowest synchronization frequency guaranteed by *DPA-Switch* is 128 kHz. Refer to Table 2 for possible combinations of the functions with example circuits shown in Figure 11 through Figure 24. A description of specific functions in terms of the LINE-SENSE pin I/V characteristic is shown in Figure 7 (right hand side). The horizontal axis represents LINE-SENSE pin current with positive polarity indicating currents flowing into the pin. The meaning of the vertical axes varies with functions. For those that control the on/off states of the output such as UV, OV and remote ON/OFF, the vertical axis represents the enable/disable states of the output. UV triggers at I_{UV} (+50 µA typical with 4 µA hysteresis) and OV triggers at I_{OV} (+135 µA typical with 4 µA hysteresis). Between the UV and OV thresholds, the output is enabled. For line feed-forward with DC_{MAX} reduction, the vertical axis represents the magnitude of the DC_{MAX} Line feed-forward with DC_{MAX} reduction lowers maximum duty cycle from 75% at $I_{L(DC)}$ (+55 µA typical) to 33% at I_{OV} (+135 µA).

EXTERNAL CURRENT LIMIT (X) Pin Operation

When current is drawn out of the EXTERNAL CURRENT LIMIT pin, it works as a voltage source of approximately 1.3 V up to a maximum current of -230 µA (typical). At -230 µA, it turns into a constant current source (refer to Figure 8).

There are two functions available through the use of the EXTERNAL CURRENT LIMIT pin: external current limit and remote ON/OFF. Shorting the EXTERNAL CURRENT LIMIT pin and SOURCE pin disables both functions. In high efficiency applications, this pin can be used to reduce the current limit externally to a value close to the operating peak current, by connecting the pin to the SOURCE pin through a resistor.

Table B. Typical LINE-SENSE and EXTERNAL CURRENT LIMIT Pin Configurations.

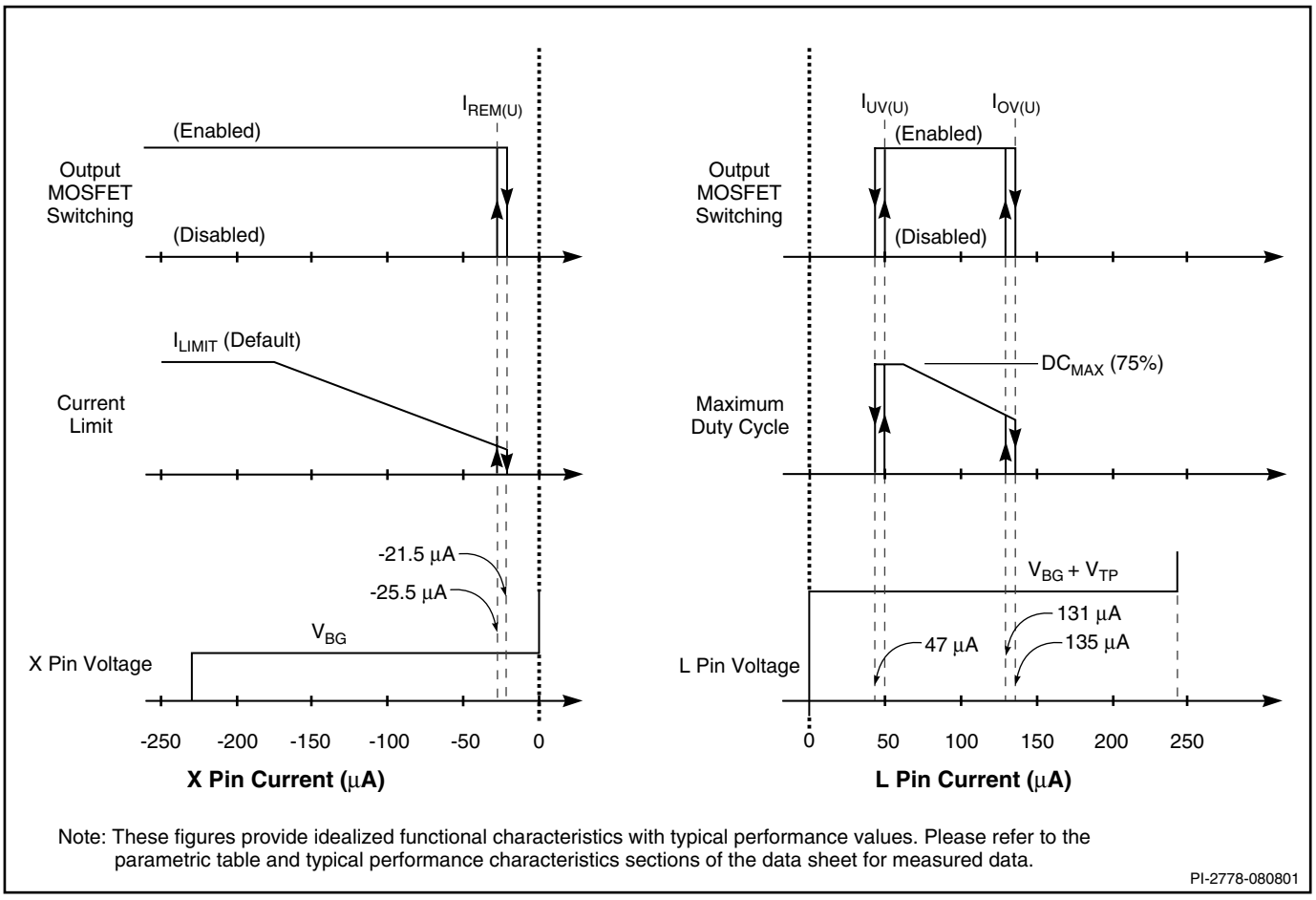


Figure 7. LINE-SENSE and EXTERNAL CURRENT LIMIT Pin Characteristics.

The pin can also be used as a remote ON/OFF control input. Table 2 shows several different ways of using this pin. See Figure 7 for a description of the functions where the horizontal axis (left hand side) represents the EXTERNAL CURRENT LIMIT pin current. The meaning of the vertical axes varies with function. For those that control the on/off states of the output such as remote ON/OFF, the vertical axis represents the enable/disable states of the output. For external

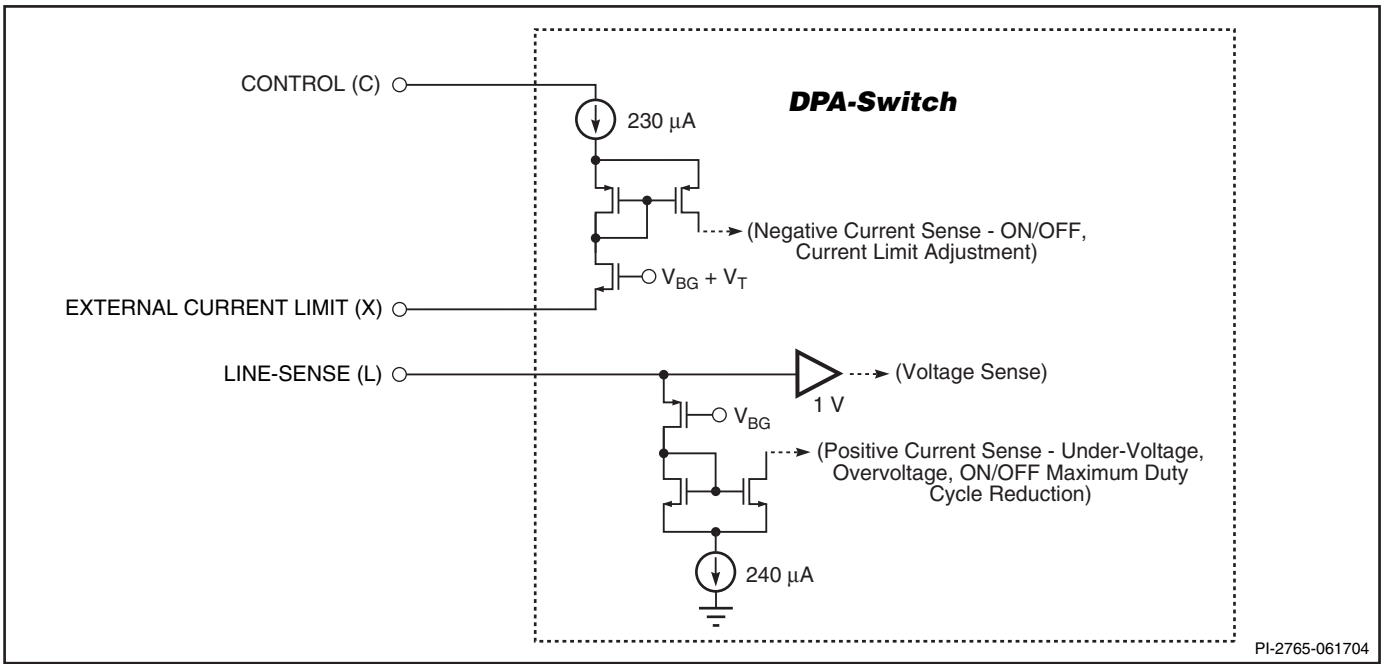


Figure 8. LINE-SENSE (L), and EXTERNAL CURRENT LIMIT (X) Pin Input Simplified Schematic.

Typical Uses of FREQUENCY (F) Pin

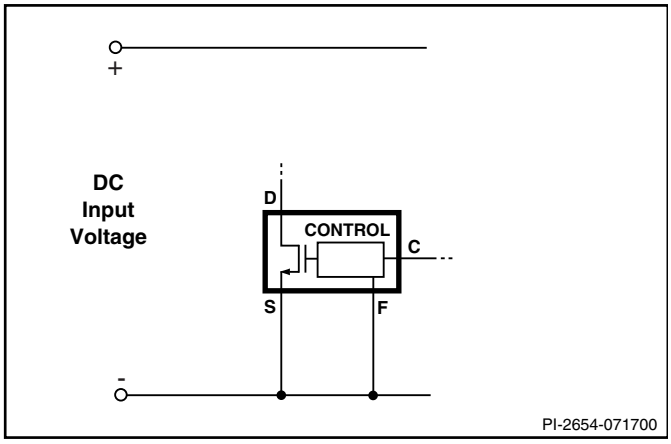


Figure 9. 400 kHz Frequency Operation.

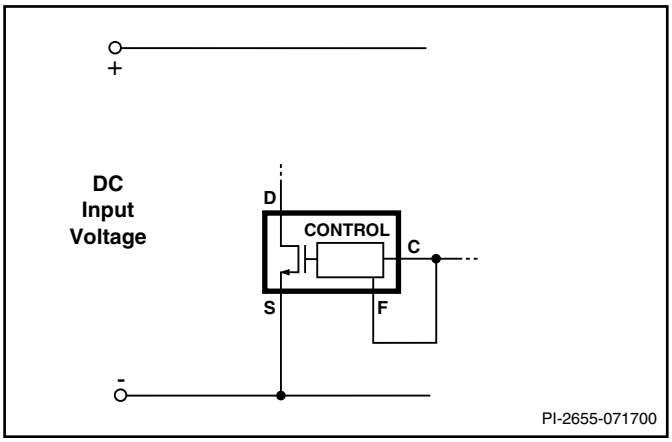


Figure 10. 300 kHz Frequency Operation.

Typical Uses of LINE-SENSE (L) and EXTERNAL CURRENT LIMIT (X) Pins

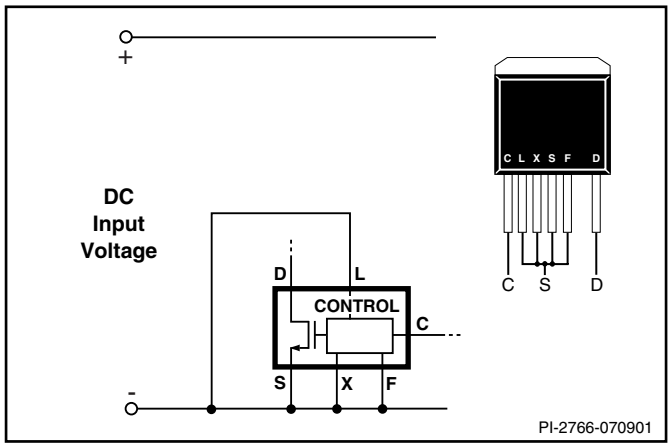


Figure 11. Three Terminal Operation (LINE-SENSE and EXTERNAL CURRENT LIMIT Features Disabled. FREQUENCY Pin can be tied to SOURCE or CONTROL Pin).

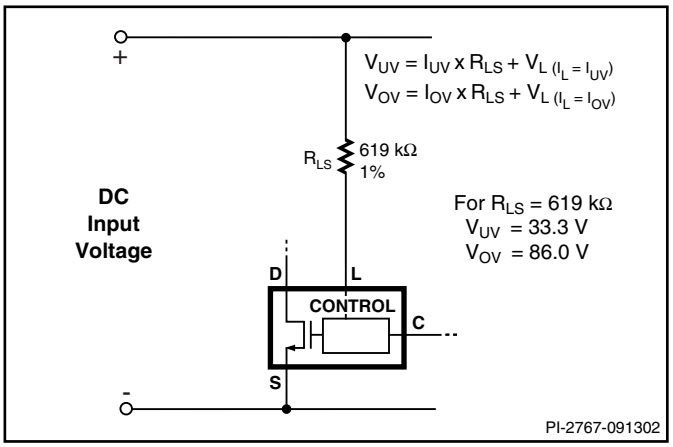


Figure 12. Line-Sensing for Under-Voltage, Overvoltage and Line Feed-forward.

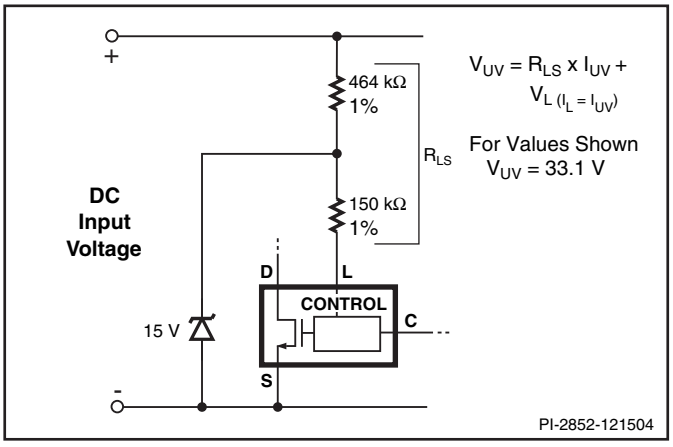


Figure 13. Line-Sensing for Under-Voltage Only (Overvoltage Disabled).

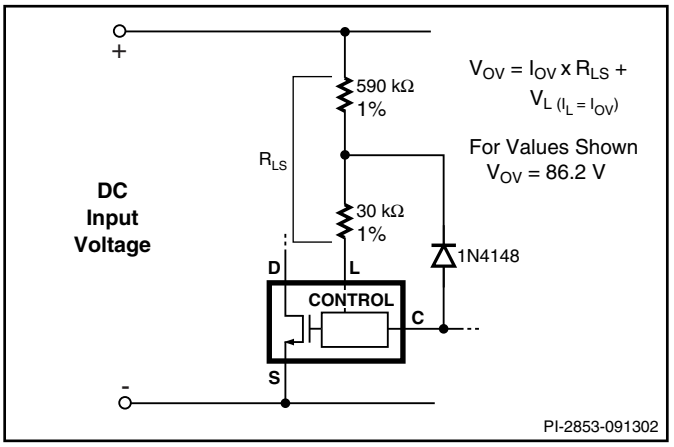


Figure 14. Line-Sensing for Overvoltage Only (Under-Voltage Disabled). Maximum Duty Cycle will be reduced at Low Line.

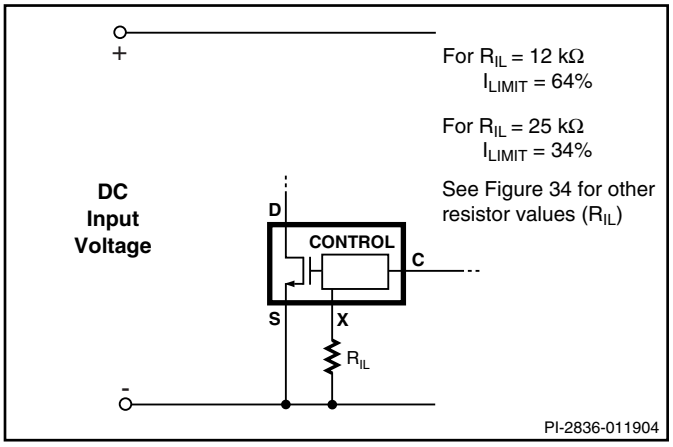


Figure 15. Externally Set Current Limit.

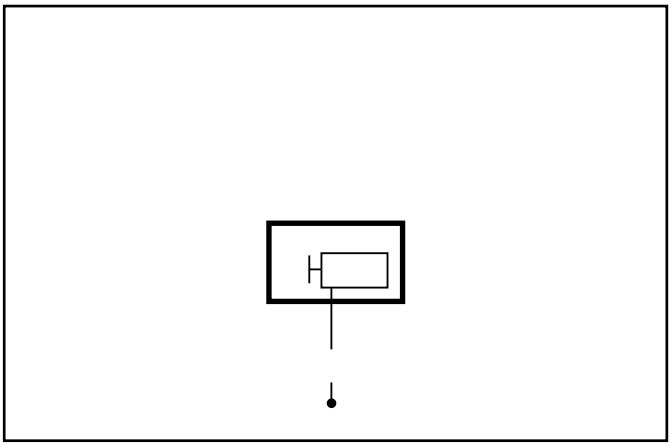


Figure 16. Current Limit Reduction with Line Voltage.

Typical Uses of LINE-SENSE (L) and EXTERNAL CURRENT LIMIT (X) Pins (cont.)

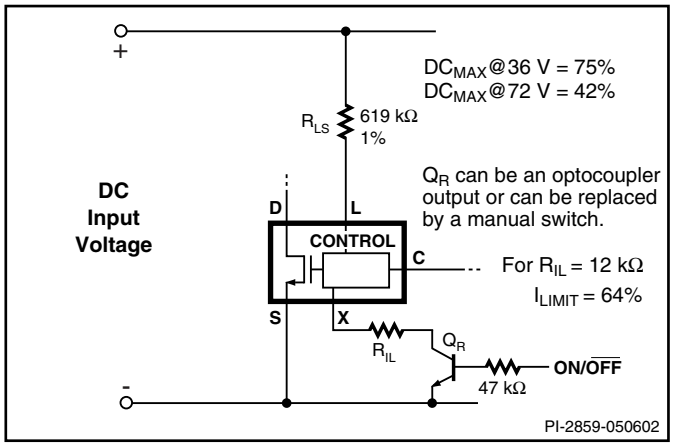


Figure 21. Active-on Remote ON/OFF with LINE-SENSE and EXTERNAL CURRENT LIMIT.

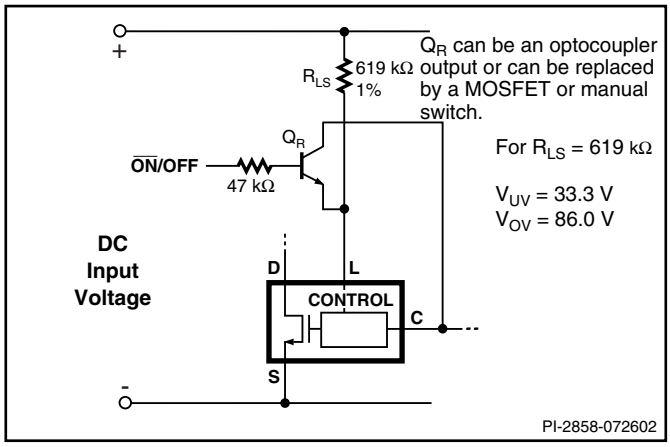


Figure 22. Active-off Remote ON/OFF with LINE-SENSE.

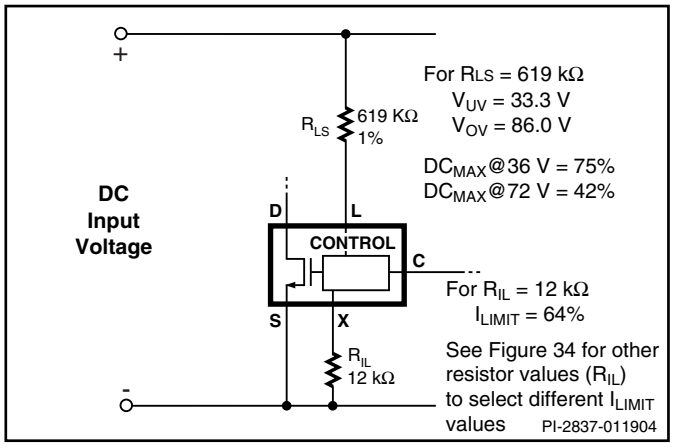


Figure 23. Line-Sensing and Externally Set Current Limit.

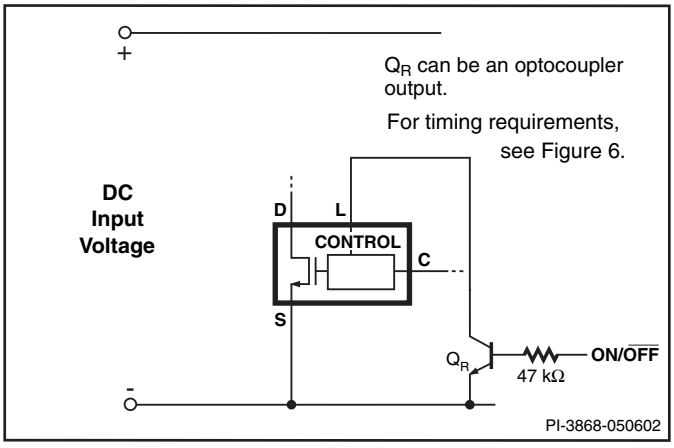


Figure 24. Synchronization.

Application Examples

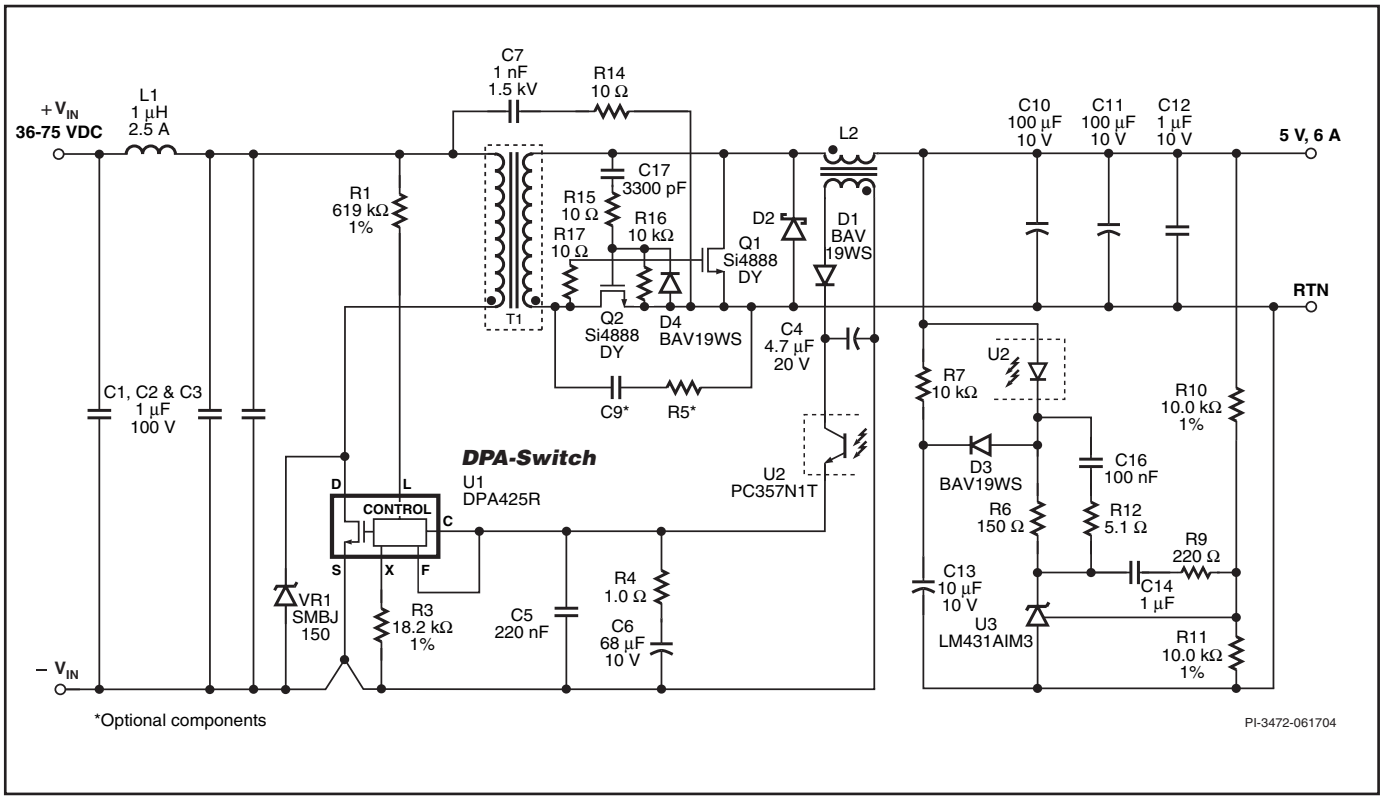


Figure 25. A High Efficiency 30 W, 5 V, Telecom Input DC-DC Converter.

High Efficiency 30 W Forward Converter

The circuit shown in Figure 25 is a typical implementation of a single output DC-DC converter using *DPA-Switch* in a forward configuration with synchronous rectification. This design delivers 30 W at 5 V, from a 36 VDC to 75 VDC input with a nominal efficiency at 48 VDC of 90% using the DPA425R.

By taking advantage of many of the built-in features of the *DPA-Switch,* the design is greatly simplified compared to a discrete implementation. Resistor R1 programs the input under-voltage and overvoltage thresholds to typically 33 V and 86 V respectively. This resistor also linearly reduces the maximum duty from the internal maximum of 75% at 36 V to 42% at 72 V to prevent core saturation during load transients at high input voltages. The *DPA-Switch* internal thresholds are toleranced and characterized so the designer can guarantee the converter will begin operation at 36 V, necessary to meet ETSI standards, without the cost of an external reference IC.

The current limit is externally set by resistor R3 to just above the drain current level needed for maximum load regulation to limit the maximum overload power of the converter. The externally programmable current limit feature also allows a larger *DPA-Switch* family member to be selected. Using the X pin, the current limit can be adjusted to the same level. A large device reduces conduction losses and improves efficiency without requiring any other circuit changes. This has been used here to replace the DPA424R with a DPA425R.

The selectable 300/400 kHz switching frequency is set to 300 kHz by connecting the FREQUENCY (F) pin to CONTROL (C).

DRAIN voltage clamping is provided by VR1, which keeps the peak DRAIN voltage within acceptable limits. Transformer core reset is provided by the gate capacitance of Q1 with R17 in series. Optional reset capacitance C9 with R5 can be added if necessary to supplement the gate capacitance of Q1.

The output of the transformer is rectified using MOSFETs to provide synchronous rectification. The UV/OV function, together with the turns ratio of the transformer, defines the maximum MOSFET gate voltage, allowing the very simple gate drive arrangement, without the need for drive windings or a drive IC. During primary on-time, capacitor C17 couples charge through resistor R15 to drive the gate of the forward MOSFET, Q2. Capacitor C17 provides a DC isolated drive for Q2, preventing gate overstress on Q1 during power down. The time constant formed by R16 and C17 is selected to be much longer than one switching cycle. Diode D4 resets the voltage on capacitor C17 before the next switching cycle. During the primary off-time, the diode D2 provides a conduction path for the energy in inductor L2 while Q1 is still off. The transformer

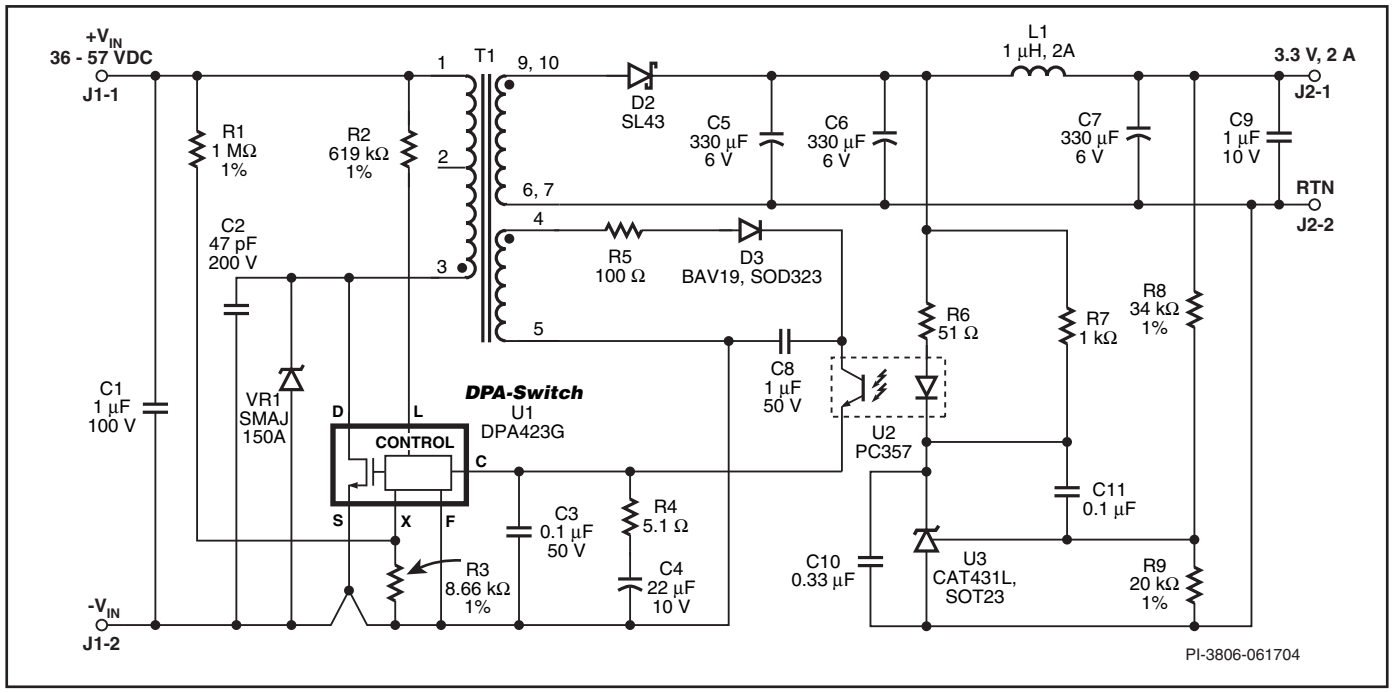


Figure 26. A Cost Effective 6.6 W, 3.3 V Flyback DC-DC Converter.

reset voltage on the secondary winding directly drives a positive voltage on the gate of catch MOSFET, Q1. MOSFET Q1 provides a low loss conduction path for a substantial portion of the primary off-time. An isolated auxiliary winding on L2, rectified and filtered by D1 and C4, provides the bias supply for the optocoupler transistor. Output regulation is achieved by using secondary side voltage reference, U3. The resistor divider formed by R10 and R11, together with the reference voltage, determines the output voltage. Diode D3 and C13 form a soft-finish network that, together with the internal duty cycle and current limit soft-start of the *DPA-Switch,* prevent output overshoot at start-up. Resistor R7 ensures that the soft-finish capacitor is discharged quickly when the output falls out of regulation. Control loop response is shaped by R6, C16, R12, C14, R9, R4 and C5, providing a wide bandwidth and good phase margin at gain crossover. Since the PWM control in *DPA-Switch* is voltage mode, no slope compensation is required for duty cycles above 50%.

Cost Effective 6.6 W Flyback Converter

The *DPA-Switch* flyback power supply provides a cost effective solution for high density PoE and VoIP DC-DC applications.

Figure 26 shows a typical implementation of a single output flyback converter using the DPA423G. For applications that require input to output isolation, this simple, low component count design delivers 6.6 W at 3.3 V from a 36 VDC to 57 VDC input with a nominal efficiency at 48 VDC of 80%.

Resistor R2 programs the input under-voltage and overvoltage thresholds to 33 V and 86 V respectively. Resistors R1 and R3 program the internal device current limit. The addition of line sense resistor R1 reduces the current limit with increasing input voltage, preventing excessive overload output current. In this design the overload output current varies less than ±2.5% across the entire input voltage range. Controlling the current limit also reduces secondary component stress and leakage inductance spikes, allowing the use of a lower V_{RRM} (30 V rather than 40 V) Schottky output diode, D2.

The primary side Zener clamp VR1 ensures the peak drain voltage is kept below the 220 V BV_{DSS} rating of U1 under input surge and overvoltage events. During normal operation, VR1 does not conduct and C2 is sufficient to limit the peak drain voltage.

The primary bias winding provides CONTROL pin current after start-up. Diode D3 rectifies the bias winding, while components R5 and C8 reduce high frequency switching noise and prevent peak charging of the bias voltage. Capacitor C3 provides local decoupling of U1 and should be physically close to the CONTROL and SOURCE pins. Energy storage for start-up and auto-restart timing is provided by C4.

The secondary is rectified by D2 and the Low ESR tantalum output capacitors, C5-C7, minimizing switching ripple and maximizing efficiency. A small footprint secondary output choke L1 and ceramic output capacitor C9 are adequate to reduce high frequency noise and ripple to below 35 mV peak-peak under full load conditions.

The output voltage is sensed by the voltage divider formed by resistors R8 and R9 and is fed to the low voltage 1.24 V reference U3. Feedback compensation is provided by R6, R7

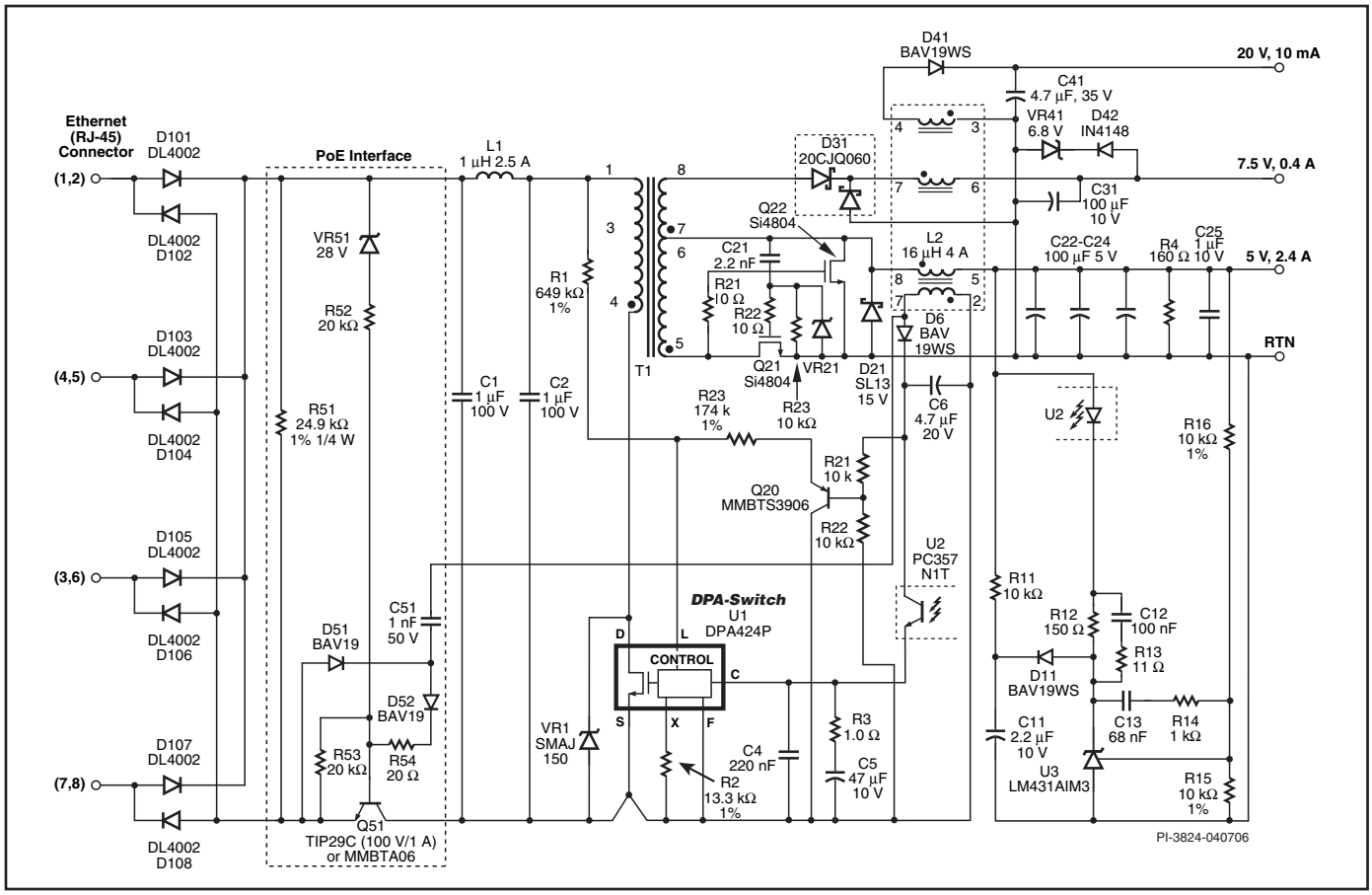


Figure 27. PoE Interface Circuit Using a Bipolar Transistor Pass-Switch and DPA424P.

and C11 together with C4 and R4. Capacitor C10 provides a soft-finish characteristic, preventing output overshoot during start-up.

Low Cost PoE VoIP Phone Converter

The basic circuitry to support IEEE standard 802.3af Power over Ethernet (PoE) is straightforward. Class 0 signature and classification circuits can be implemented with a single resistor and the required under-voltage lockout function is a voltage controlled pass-switch. By adding this circuitry to the front end of a DPA converter, a low cost and low component count PoE powered device (PD) power supply can be implemented. Figure 27 shows a typical PD solution.

The PoE specification requires the PD to provide three fundamental functions: discovery, classification, and pass-switch connection.

When input voltage is applied to the PD, it must present the correct discovery signature impedance in the voltage range of 2.5 VDC to 10 VDC. This impedance is provided by R51 in Figure 27.

The second “classification” phase occurs at input voltages 15 VDC to 20 VDC. The PD must draw a specified current to identify the device class (Class 0 specifies 0.5 mA to 4 mA). This is again accomplished by resistor R51.

In the third phase, the bipolar pass-switch (Q51 in Figure 27) connects the input voltage to the power supply at voltages above approximately 30 VDC (28 V+VR52). Zener diode VR51 conducts, driving the current through resistor R52 to the base of Q51. Resistor R53 prevents turn-on under other conditions. Once the Power supply has started, components D51, D52, C51 and R54 enhance the base-current drive by coupling power from the power supply bias winding.

Once the three start up phases have been successfully completed, the *DPA-Switch* is allowed to function as a forward converter (described in Figure 25 and accompanying text).

Key Application Considerations

DPA-Switch Design Considerations

Power Table

This section provides a description of the assumptions used to generate the power tables (Tables 1 and 3 through 6) and explains how to use the information provided by them.

All Power tables: Tables 1 and 3 through 6

- Maximum output power is limited by the device internal current limit. This is the peak output power which could become the continuous output power, provided adequate heat sinking is used.
- Data assumes adequate heat sinking to keep the junction temperature at or below 100 °C and worst case $R_{DS(ON)}$ at T_J = 100 °C.
- The use of P and G packages are recommended for device dissipation equal to or less than 1.5 W only due to package thermal limitation. For device dissipation above 1.5 W, use S and R packages.

Forward power tables: Tables 1 (upper half), 3 and 4

- Output power figures are based on forward topology using Schottky diode rectification. Up to 5% higher output power is possible using synchronous rectification.
- Dissipation data assumes a diode loss representing 6% of the total output power and combined loss in magnetic components representing 6% of the total output power. *DPA-Switch* losses are based on a ratio between conduction and switching losses of approximately 3:1. These assumptions are typical for a single 5 V output forward converter design using Schottky rectification and adequately designed magnetic components.

Flyback power tables: Tables 1 (lower half), 5 and 6

- Output power and dissipation figures are based on a 5 V output using Schottky diode rectification with an efficiency of 85%. Values are generated by calculation based on $I^2 \cdot R_{DS(ON)}$ losses and characterization of switching losses, correlated to bench measurement of each *DPA-Switch* device.
- Device dissipations above 1.5 W are possible using the S and R packages. However the forward converter topology is recommended for such higher power designs.

The power tables provide two types of information. The first is the expected device dissipation for a given output power. The second is the maximum power output. Each table specifies the input voltage range and assumes a single 5 V output using Schottky diode rectification.

For example, referring to Table 1, for 36 VDC to 75 VDC input range, DPA424 would typically dissipate 1 W in a 23 W forward converter and has a maximum power capacity of 35 W. In the

OUTPUT POWER TABLE						
16-32 VDC RANGE (FORWARD)[2]						
Total Device Dissipation / PRODUCT[3]	0.5 W	1 W	2.5 W	4 W	6 W	Max Power Output[1]
DPA422	3.5 W	4.5 W	-	-	-	5.0 W
DPA423	5 W	7 W	-	-	-	7.5 W
DPA424	7 W	10 W	15 W	-	-	15.5 W
DPA425	10 W	14 W	22 W	27 W	-	31 W
DPA426	12 W	16.5 W	25 W	31 W	37 W	43 W

Table 3. Output Power Table for 16-32 VDC Input Voltage. Notes: 1. Limited by device internal current limit. 2. See text in this section for a complete description of assumptions. 3. See Part Ordering Information.

OUTPUT POWER TABLE						
24-48 VDC RANGE (FORWARD)[2]						
Total Device Dissipation / PRODUCT[3]	0.5 W	1 W	2.5 W	4 W	6 W	Max Power Output[1]
DPA422	5.5 W	7 W	-	-	-	8 W
DPA423	8 W	11 W	-	-	-	11.5 W
DPA424	11 W	16 W	23.5 W	-	-	25 W
DPA425	16 W	22 W	35 W	43 W	-	47 W
DPA426	18 W	25 W	39 W	48 W	58 W	65 W

Table 4. Output Power Table for 24-48 VDC Input Voltage (See Table 3 for Notes).

OUTPUT POWER TABLE					
16-32 VDC RANGE (FLYBACK)[2]					
Total Device Dissipation / PRODUCT[3]	0.5 W	0.75 W	1 W	1.5 W	Max Power Output[1]
DPA422	3 W		-	-	4.5 W
DPA423	5 W	-	-	-	6 W
DPA424	6.5 W	8.5 W	10 W	-	11 W
DPA425	7 W	10 W	12 W	15 W	22 W

Table 5. Flyback Output Power Table for 16-32 VDC Input Voltage (See Table 3 for Notes).

OUTPUT POWER TABLE					
24-48 VDC RANGE (FLYBACK)[2]					
Total Device Dissipation / PRODUCT[3,4]	0.5 W	0.75 W	1 W	1.5 W	Max Power Output[1]
DPA422	5 W		-	-	7 W
DPA423	7 W	-	-	-	8.5 W
DPA424	8.5 W	11.5 W	14 W	-	17 W

Table 6. Flyback Output Power Table for 24-48 VDC Input Voltage. Notes: 1. Maximum output power is limited by device internal current limit. 2. See text in this section for a complete description of assumptions. 3. See Part Ordering Information. 4. Higher switching losses may prevent DPA425 from delivering more power than a smaller device.

same converter, DPA425 would dissipate 0.5 W. Selecting DPA425 with associated reduced dissipation would increase overall converter efficiency by approximately 2%.

Issues Affecting Dissipation:

1) Using synchronous rectification will tend to reduce device dissipation.
2) Designs with lower output voltages and higher currents will tend to increase the device dissipation listed in the power table.
3) Reduced input voltage decreases the available output power for the same device dissipation. Tables 3 to 6 are the power tables for 16 VDC and 24 VDC input voltages. Input voltages below 16 V are possible, but since the internal start-up current source is not specified at voltages below 16 V, an external chip supply current should be fed into the CONTROL pin approximately equal to but less than I_{CD1}.

***DPA-Switch* Selection**

Use Tables 1 and 3 through 6 to select the *DPA-Switch* based on device dissipation. Selecting the optimum *DPA-Switch* depends upon required maximum output power, efficiency, heat sinking constraints and cost goals. With the option to externally reduce current limit, a larger *DPA-Switch* may be used for lower power applications where higher efficiency is needed or minimal heat sinking is available. Generally, selecting the next larger device, than is required for power delivery will give the highest efficiency. Selecting even larger devices may give little or no improvement in efficiency due to the improvement in conduction losses being negated by larger device switching losses. Figure 50 provides information on switching losses. This together with conduction loss calculations give an estimate of device dissipation.

Primary Clamp

A primary clamp network is recommended to keep the peak DRAIN voltage due to primary leakage inductance to below the BV_{DSS} specification. A Zener diode combined with a small value capacitor connected across the primary winding is a low cost and low part count implementation.

Output Rectification

Rectification of the secondary is typically performed using Schottky diodes or synchronous rectification. Schottky diodes are selected for peak inverse voltage, output current, forward drop and thermal conditions. Synchronous rectification requires the additional complication of providing gate drive. The specified line under-voltage and line overvoltage thresholds of *DPA-Switch* simplifies deriving gate drive directly from the transformer secondary winding for many applications. The turns ratio of the transformer together with the under/overvoltage thresholds defines the minimum and maximum gate voltages, removing the need for Zeners to clamp the gate voltage.

Soft-Start

Generally a power supply experiences maximum stress at start-up before the feedback loop achieves regulation. For a period of 5 ms the on-chip soft-start linearly increases the duty cycle from zero to the default DC_{MAX} at turn-on. In addition, the primary current limit increases from 85% to 100% over the same period. This causes the output voltage to rise in an orderly manner allowing time for the feedback loop to take control of the duty cycle. This integrated soft-start reduces the stress on the *DPA-Switch* MOSFET, clamp circuit and output diode(s), and helps prevent transformer saturation during start-up. Also, soft-start limits the amount of output voltage overshoot, and in many applications eliminates the need for a soft-finish capacitor. If necessary, to remove output overshoot, a soft-finish capacitor may be added to the secondary reference.

Switching Frequency

The FREQUENCY pin of *DPA-Switch* offers a switching frequency option of 400 kHz or 300 kHz. Operating at 300 kHz will increase the amount of magnetization energy stored in the transformer. This is ideal for applications using synchronous rectification driven directly from the transformer secondary where this energy can be used to drive the catch MOSFET gate.

Transformer Design

It is recommended that the forward converter transformer be designed for maximum operating flux swing of 1500 Gauss and a peak flux density of 3500 Gauss. When operating at the maximum current limit of the selected *DPA-Switch* (during overload conditions), neither magnetic component (transformer and output inductor) should be allowed to saturate. When a larger device than necessary has been selected, reducing the internal current limit close to the operating peak current limits overload power and minimizes the size of the secondary components.

No-load and Standby Consumption

Cycle skipping operation at light or no load can significantly reduce power loss. In addition this operating mode ensures that the output maintains regulation even without an external minimum load. However, if cycle skipping is undesirable in a particular application, it can be avoided by adding sufficient pre-load.

DPA-Switch Layout Considerations

The *DPA-Switch* can operate with large DRAIN current, the following guidelines should be carefully followed.

Primary Side Connections

The tab of *DPA-Switch* R package and S-PAK is the intended return path for the high switching currents. Therefore, the tab should be connected by wide, low impedance traces back to

the input decoupling capacitor. The SOURCE pin should not be used to return the power currents; incorrect operation of the device may result. The SOURCE is only intended as a signal ground. The device tab (SOURCE) is the correct connection for high current with the R package and S-PAK.

The CONTROL pin bypass capacitor should be located as close as possible to the SOURCE and CONTROL pins and its SOURCE connection trace should not be shared by the main MOSFET switching currents. All SOURCE pin referenced components connected to the LINE-SENSE or EXTERNAL CURRENT LIMIT pins should also be located closely between their respective pin and SOURCE. Once again, the SOURCE connection trace of these components should not be shared by the main MOSFET switching currents. It is critical that the tab (SOURCE) power switching currents are returned to the input capacitor through a separate trace that is not shared by the components connected to CONTROL, LINE-SENSE or EXTERNAL CURRENT LIMIT pins.

Any traces to the L or X pins should be kept as short as possible and away from the DRAIN trace to prevent noise coupling. LINE-SENSE resistor (R1 in Figure 25) should be located close to the L pin to minimize the trace length on the L pin side.

In addition to the CONTROL pin capacitor (C6 in Figure 25), a high frequency bypass capacitor in parallel is recommended as close as possible between SOURCE and CONTROL pins for better noise immunity. The feedback optocoupler output should also be located close to the CONTROL and SOURCE pins of *DPA-Switch*.

Heat Sinking

To maximize heat sinking of the *DPA-Switch* S, R or G package and the other power components, special thermally conductive PC board material (aluminum clad PC board) is recommended. This has an aluminum sheet bonded to the PC board during the manufacturing process to provide heat sinking directly and allow the attachment of an external heat sink. If normal PC board material is used (such as FR4), providing copper areas on both sides of the board and using thicker copper will improve heat sinking.

If an aluminum clad board is used then shielding of switching nodes is recommended. This consists of an area of copper placed directly underneath switching nodes such as the drain node, and output diode to provide an electrostatic shield to prevent coupling to the aluminum substrate. These areas are connected to input negative in the case of the primary and output return for secondary. This reduces the amount of capacitive coupling into the insulated aluminum substrate that can then appear on the output as ripple and high frequency noise.

Quick Design Checklist

As with any power supply design, all *DPA-Switch* designs should be verified on the bench to make sure that component specifications limits are not exceeded under worst case conditions. The following minimum set of tests for *DPA-Switch* forward converters is strongly recommended:

1. Maximum drain voltage – Verify that peak V_{DS} does not exceed minimum BV_{DSS} at highest input voltage and maximum overload output power. It is normal, however, to have additional margin of approximately 25 V below BV_{DSS} to allow for other power supply component unit-to-unit variations. Maximum overload output power occurs when the output is loaded to a level just before the power supply goes into auto-restart (loss of regulation).

2. Transformer reset margin – Drain voltage should also be checked at highest input voltage with a severe load step (50-100%) to verify adequate transformer reset margin. This test shows the duty cycle at high input voltage, placing the most demand on the transformer reset circuit.

3. Maximum drain current – At maximum ambient temperature, maximum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of transformer or output inductor saturation and excessive leading edge current spikes. *DPA-Switch* has a leading edge blanking time of 100 ns to prevent premature termination of the on cycle. Verify that the leading edge current spike does not extend beyond the blanking period.

4. Thermal check – At maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specifications are not exceeded for the transformer, output diodes, output choke(s) and output capacitors. The *DPA-Switch* is fully protected against over-temperature conditions by its thermal shutdown feature. It is recommended that sufficient heat sinking is provided to keep the tab temperature at or below 115 °C (S and R packages), SOURCE pins at or below 100 °C (P/G packages) under worst case continuous load conditions (at low input voltage, maximum ambient and full load). This provides adequate margin to minimum thermal shutdown temperature (130 °C) to account for part-to-part $R_{DS(ON)}$ variation. When monitoring device temperatures, note that the junction-to-case thermal resistance should be accounted for when estimating die temperature.

Design Tools

Up-to-date information on design tools is available at the Power Integrations website: *www.powerint.com*.

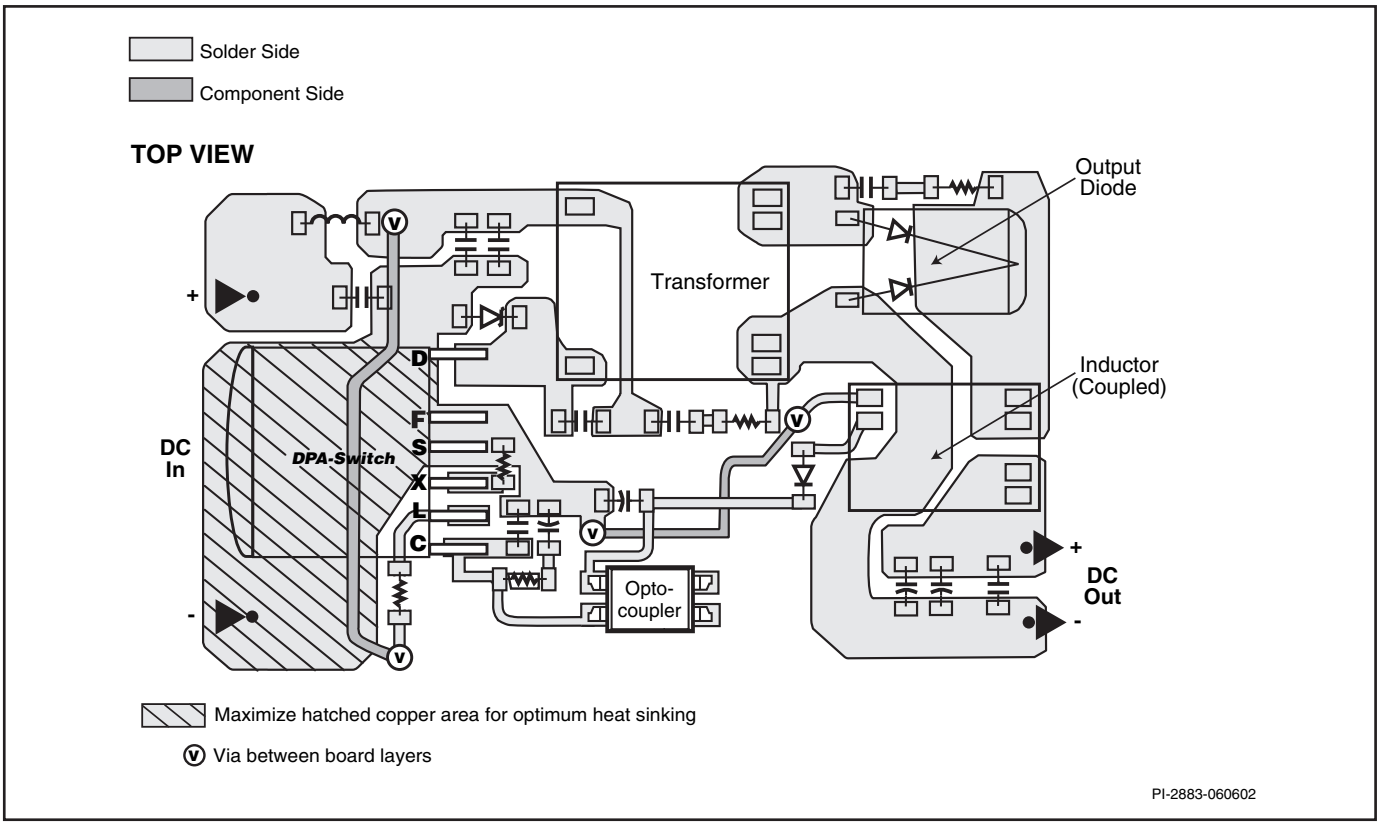


Figure 28. Layout Considerations for DPA-Switch Using S-PAK or R Package.

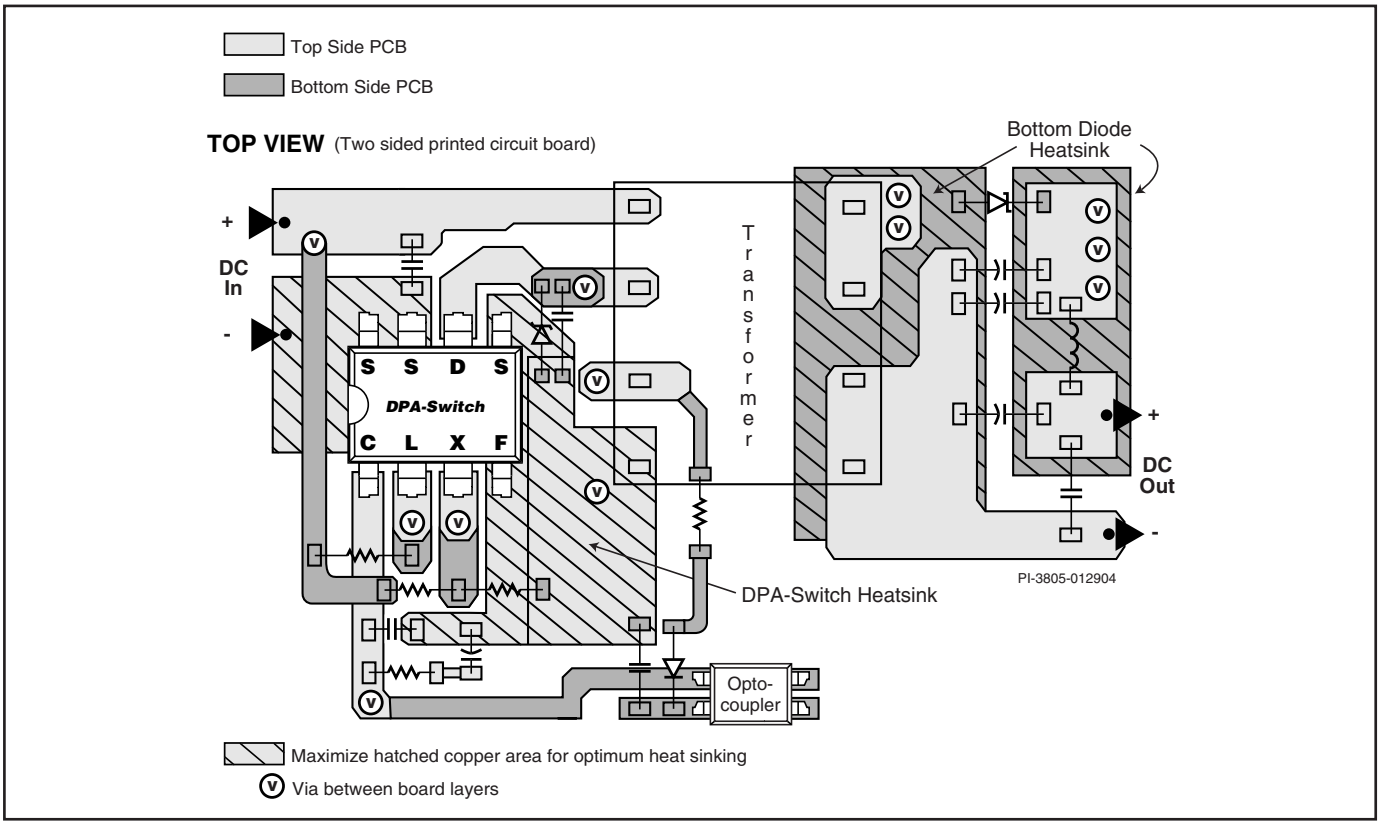


Figure 29. Layout Considerations for DPA-Switch Using G Package.

ABSOLUTE MAXIMUM RATINGS[1,4]

DRAIN Voltage ..... -0.3 V to 220 V
DRAIN Peak Current: DPA422..... 1.31 A
DPA423..... 1.75A
DPA424..... 3.5 A
DPA425..... 7A
DPA426..... 9.6 A
CONTROL Voltage ..... -0.3 V to 9 V
CONTROL Current ..... 100 mA
LINE SENSE Pin Voltage ..... -0.3 V to 9 V
EXTERNAL CURRENT LIMIT Pin Voltage ..... -0.3 V to 9 V
FREQUENCY Pin Voltage ..... -0.3 V to 9 V
Storage Temperature -65 °C to 150 °C
Operating Junction Temperature[2] ..... -40 °C to 150 °C
Lead Temperature[3] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.
4. Maximum ratings specified may be applied, one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

THERMAL IMPEDANCE

Thermal Impedance: P or G Package:
(θ_{JA}) ..... 70 °C/W[1]; 60 °C/W[2]
(θ_{JC})[3] ..... 11 °C/W
R Package:
(θ_{JA}) ..... 40 °C/W[4]
(θ_{JA}) ..... 30 °C/W[5]
(θ_{JC})[6] ..... 2 °C/W
S-PAK:
(θ_{JA}) ..... 49 °C/W[4]
(θ_{JA}) ..... 39 °C/W[5]
(θ_{JC})[6] ..... 2 °C/W

Notes:
1. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
2. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Measured on pin 7 (SOURCE) close to plastic interface.
4. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.
5. Soldered to 3 sq. in. (1935 mm^2), 2 oz. (610 g/m^2) copper clad.
6. Measured at the back surface of tab.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 33 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Switching Frequency	f_{OSC}	T_J = 25 °C	FREQUENCY Pin Connected to SOURCE	375	400	425	kHz
			FREQUENCY Pin Connected to CONTROL	282	300	317	
Duty Cycle (Prior to Cycle Skipping)	DC_{MIN}				4	6	%
Maximum Duty Cycle	DC_{MAX}	$I_C = I_{CD1}$	V_L = 0 V	71	75	79	%
			I_L = 80 µA	52	62	71	
			I_L = 115 µA	32	42	57	
Control Current at Start of Cycle Skipping	$I_{C(skip)}$	T_J = 25 °C; f_{OSC} = 400 kHz	DPA422		6.3	8.0	mA
			DPA423		7.2	9.0	
			DPA424		8.2	10.0	
			DPA425		10.0	12.0	
			DPA426		11.5	14.0	
External Bias Current	I_B	T_J = 25 °C; f_{OSC} = 400 kHz	DPA422	1.8	2.5	3.1	mA
			DPA423	2	2.8	3.5	
			DPA424	2.5	3.5	4.4	
			DPA425	3.6	4.8	6.0	
			DPA426	4.4	5.7	7.1	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 33 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS (cont.)							
Softstart Time	t_{SOFT}	T_J = 25 °C; DC_{MIN} to DC_{MAX}			5	7.2	ms
PWM Gain	DC_{reg}	T_J = 25 °C; $I_C = (I_{C(skip)} + I_B)/2$		-28	-22	-18	%/mA
PWM Gain Temperature Drift		See Note A			-0.01		%/mA/°C
Dynamic Impedance	Z_C	T_J = 25 °C; $I_C = (I_{C(skip)} + I_B)/2$		10	15	22	Ω
Dynamic Impedance Temperature Drift					0.18		%/°C
CONTROL Pin Internal Filter Pole					30		kHz
SHUTDOWN/AUTO-RESTART							
CONTROL Pin Charging Current	$I_{C(CH)}$	During Startup and Auto-Restart: V_C = 5.0 V; V_D = 16 V & 40 V; T_J = 25 °C		-5.2	-4	-3	mA
		Average Current at the Beginning of Softstart: V_C = 5.0 V; V_D = 16 V & 40 V; T_J = 25 °C			-19		
Charging Current Temperature Drift		See Note A			-0.6		%/°C
Auto-Restart Upper Threshold Voltage	$V_{C(AR)U}$				5.8		V
Auto-Restart Lower Threshold Voltage	$V_{C(AR)L}$			4.5	4.8	5.1	V
Auto-Restart Hysteresis Voltage	$V_{C(AR)Hyst}$			0.8	1		V
Auto-Restart Duty Cycle	$DC_{(AR)}$	$C_{CONTROL}$ = 22 µF; f_{OSC} = 400 kHz; V_X = 0 V				10	%
Auto-Restart Frequency	$f_{(AR)}$	$C_{CONTROL}$ = 22 µF; f_{OSC} = 400 kHz; V_X = 0 V			3.8		Hz
LINE-SENSE (L) AND EXTERNAL CURRENT LIMIT (X) INPUTS							
Line Under-Voltage Threshold Current and Hysteresis (L Pin)	I_{UV}	T_J = 25 °C	Threshold from Off to On	48	50	52	µA
			Threshold from On to Off	44.5	47	49.5	
			Hysteresis	2	3		

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 33 (Unless Otherwise Specified)		Min	Typ	Max	Units
LINE-SENSE (L) AND EXTERNAL CURRENT LIMIT (X) INPUTS (cont.)							
Line Overvoltage or Remote ON/ OFF Threshold Current and Hysteresis (L Pin)	I_{OV}	T_J = 25 °C	Threshold from On to Off		135	149	µA
			Threshold from Off to On	117	131		
			Hysteresis		4		
Remote ON/OFF Negative Threshold Current and Hysteresis (X Pin)	I_{REM}	T_J = 25 °C	Threshold from On to Off	-27	-21.5	-16	µA
			Threshold from Off to On		-25.5		
			Hysteresis		4.5		
L Pin Short Circuit Current	$I_{L(SC)}$	$V_L = V_C$		175	240	380	µA
		V_L = 0 V		-230	-170		
X Pin Short Circuit Current	$I_{X(SC)}$	V_X = 0 V	Normal Mode	-270	-230	-185	µA
			Remote OFF using L Pin	-105	-85	-65	
Line Pin Voltage (Positive Current)	V_L	$I_L = I_{UV}$		2.05	2.35	2.6	V
		$I_L = I_{OV}$		2.1	2.5	2.9	
X Pin Voltage (Negative Current)	V_X	I_X = -50 µA			1.35		
		I_X = -150 µA			1.25		
Maximum Duty Cycle Reduction Onset Threshold Current	$I_{L(DC)}$	T_J = 25 °C			55		µA
Remote OFF DRAIN Supply Current	$I_{D(RMT)}$	V_D = 40 V V_X = 0 V	V_L = Floating		0.6	1.1	mA
			$V_L = V_C$		0.9	1.5	
L Pin Voltage Turn-On Threshold in Synchronous Mode	$V_{L(TH)}$			0.6	1	1.4	V
On-Time Pulse Width for Synchronization	$t_{on(sync)}$	f_{OSC} = 400 kHz		120		2250	ns
		f_{OSC} = 300 kHz		120		3080	
Off-Time Pulse Width for Synchronization	$t_{off(sync)}$			0.25		7.7	µs
Synchronous Turn-On Delay	$t_{delay(sync)}$	From Synchronous On to Drain Turn-On				250	ns

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 33 (Unless Otherwise Specified)		Min	Typ	Max	Units
FREQUENCY (F) INPUT							
FREQUENCY Pin Threshold Voltage	V_F			1.1		4	V
FREQUENCY Pin Input Current	I_F	V_F = 0 V			-0.38		µA
		$V_F = V_C$			17	120	
FREQUENCY Pin Delay Time	$t_{delay(VF)}$					2	µs
CIRCUIT PROTECTION							
Self Protection Current Limit (See Note B)	I_{LIMIT}	T_J = 25 °C	DPA422 di/dt = 225 mA/µs	0.86	0.935	1.0	A
			DPA423 di/dt = 300 mA/µs	1.16	1.25	1.34	
			DPA424 di/dt = 600 mA/µs	2.32	2.50	2.68	
			DPA425 di/dt = 1.25 A/µs	4.65	5.00	5.35	
			DPA426 di/dt = 1.75 A/µs	6.50	7.00	7.50	
Initial Current Limit	I_{INIT}	V_D = 35 V		0.9 x $I_{LIMIT(min)}$			A
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C				100	ns
Current Limit Delay	$t_{IL(D)}$	$I_C = (I_{C(skip)} + I_B)/2$			100		ns
Thermal Shut-down Temperature	$T_{J(SD)}$			130	137	145	°C
Thermal Shut-down Hysteresis	$T_{J(SD)hyst}$				27		°C
Power-Up Reset Threshold Voltage	$V_{C(RESET)}$			1.5	2.75	4	V
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	DPA422 I_D = 150 mA	T_J = 25 °C		2.60	3.00	Ω
			T_J = 100 °C		4.00	4.60	
		DPA423 I_D = 300 mA	T_J = 25 °C		1.30	1.50	
			T_J = 100 °C		2.00	2.30	
		DPA424 I_D = 600 mA	T_J = 25 °C		0.65	0.75	
			T_J = 100 °C		1.00	1.15	
		DPA425 I_D = 1.25 A	T_J = 25 °C		0.33	0.38	
			T_J = 100 °C		0.50	0.58	
		DPA426 I_D = 1.75 A	T_J = 25 °C		0.24	0.28	
			T_J = 100 °C		0.37	0.43	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 33 (Unless Otherwise Specified)		Min	Typ	Max	Units
OUTPUT (cont.)							
OFF-State Drain Leakage Current	I_{DSS}	V_X, V_L = Floating; V_D = 150 V; T_J = 125 °C; $I_C = (I_{C(skip)} + I_B)/2$	DPA422			33	µA
			DPA423			65	
			DPA424			130	
			DPA425			260	
			DPA426			360	
Breakdown Voltage	BV_{DSS}	V_X, V_L = Floating; T_J = 25 °C; $I_C = (I_{C(skip)} + I_B)/2$; See Note C		220			V
Rise Time	t_R	Measured in a Typical Application			10		ns
Fall Time	t_F	Measured in a Typical Application			10		ns
SUPPLY VOLTAGE CHARACTERISTICS							
DRAIN Supply Voltage		See Note D		16			V
Shunt Regulator Voltage	$V_{C(SHUNT)}$	$I_C = (I_{C(skip)} + I_B)/2$: T_J = 25 °C		5.6	5.85	6.0	V
Shunt Regulator Temperature Drift		$I_C = (I_{C(skip)} + I_B)/2$			±50		PPM/°C
CONTROL Supply/Discharge Current	I_{CD1}	Output MOSFET Enabled V_L = 0 V; f_{OSC} = 400 kHz	DPA422	1.6	2.0	2.4	mA
			DPA423	1.9	2.3	2.7	
			DPA424	2.6	3.0	3.4	
			DPA425	3.7	4.3	4.8	
			DPA426	4.8	5.4	6	
	I_{CD2}	Output MOSFET Disabled V_L = 0 V; f_{OSC} = 400 kHz		0.4	0.73	1.2	

NOTES:

A. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

B. For externally adjusted current limit values, please refer to Figure 35 (Current Limit vs. External Current Limit Resistance) in the Typical Performance Characteristics section.

C. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping the DRAIN pin voltage up to but not exceeding minimum BV_{DSS}.

D. It is possible to start up and operate *DPA-Switch* at DRAIN voltages well below 16 V. However, the CONTROL pin charging current is reduced, which affects start-up time, auto-restart frequency, and auto-restart duty cycle. Refer to Figure 45, the characteristic graph on CONTROL pin charge current (I_C) vs. DRAIN voltage for low voltage operation characteristics.

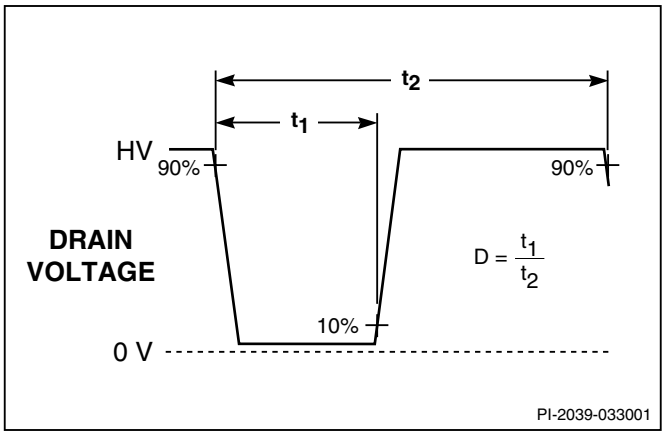


Figure 30. Duty Cycle Measurement.

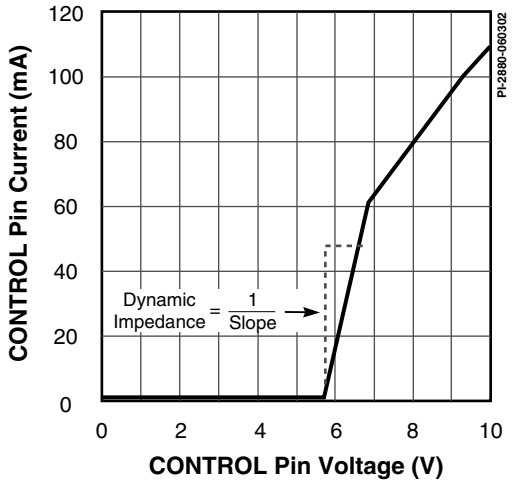


Figure 31. CONTROL Pin I-V Characteristic.

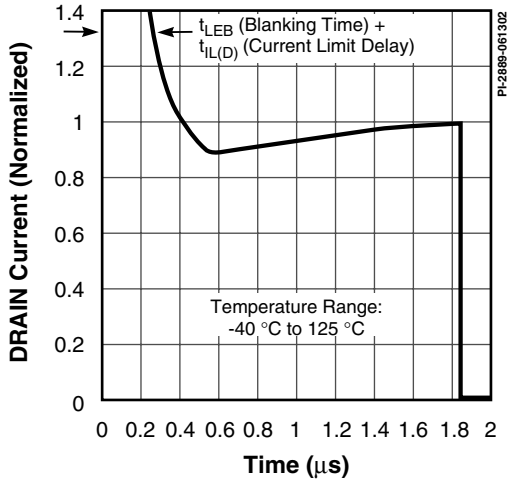


Figure 32. Typical Drain Operation Current Envelope.

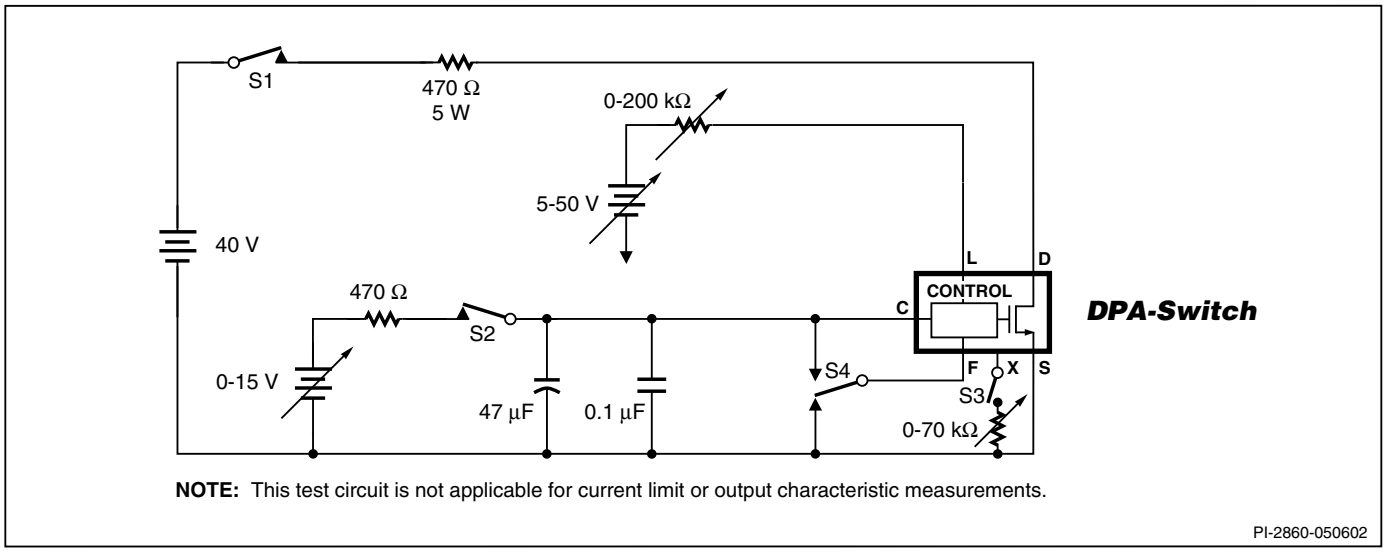


Figure 33. DPA-Switch General Test Circuit.

BENCH TEST PRECAUTIONS FOR EVALUATION OF ELECTRICAL CHARACTERISTICS

The following precautions should be followed when testing *DPA-Switch* by itself outside of a power supply. The schematic shown in Figure 33 is suggested for laboratory testing of *DPA-Switch*.

When the DRAIN pin supply is turned on, the part will be in the auto-restart mode. The CONTROL pin voltage will be oscillating at a low frequency between 4.8 V and 5.8 V and the drain is turned on every eighth cycle of the CONTROL pin oscillation. If the CONTROL pin power supply is turned on while in this auto-restart mode, there is only a 12.5% chance that the CONTROL pin oscillation will be in the correct state (drain active state) so that the continuous drain voltage waveform may be observed. It is recommended that the V_C power supply be turned on first and the DRAIN pin power supply second if continuous drain voltage waveforms are to be observed. The 12.5% chance of being in the correct state is due to the divide-by-8 counter. Temporarily shorting the CONTROL pin to the SOURCE pin will reset *DPA-Switch*, which then will come up in the correct state.

Typical Performance Characteristics

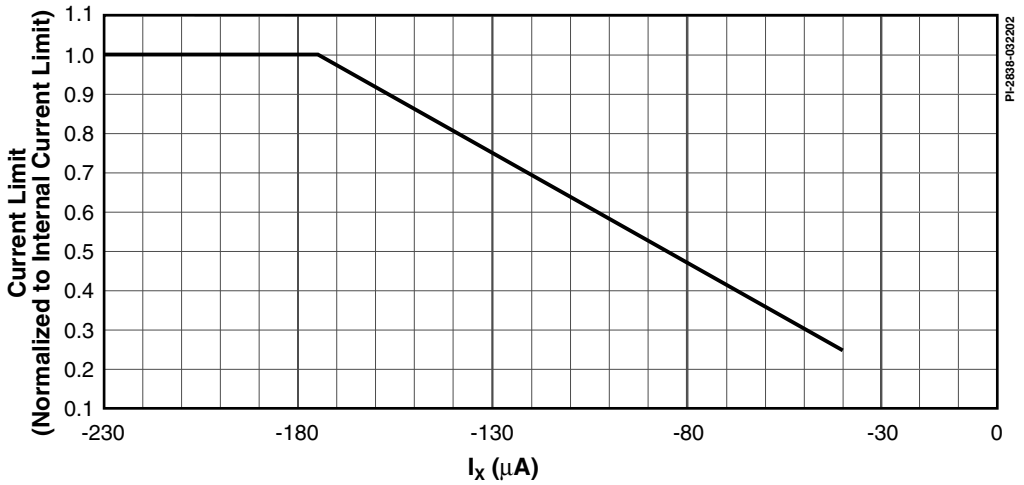


Figure 34. Current Limit vs. EXTERNAL CURRENT LIMIT Pin Current.

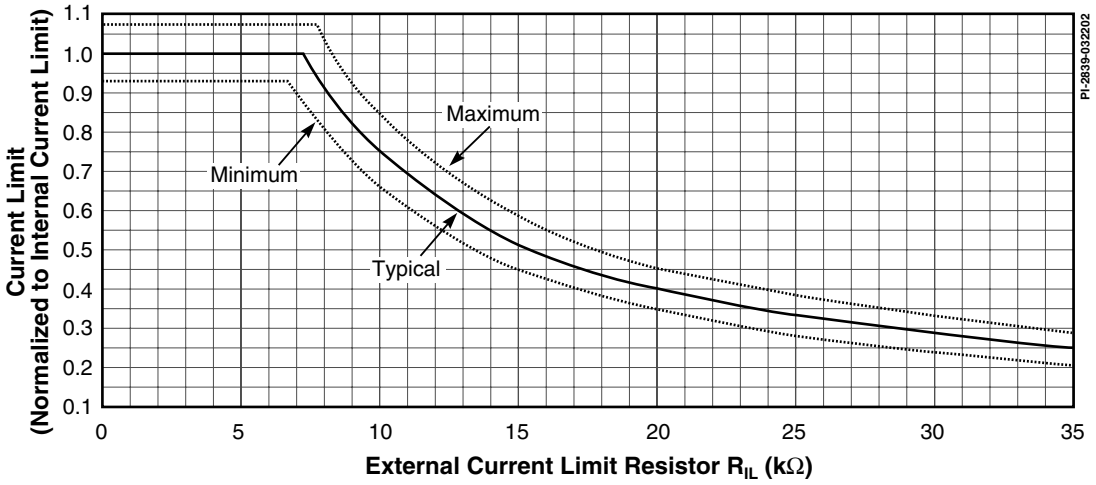


Figure 35. Current Limit vs. External Current Limit Resistance.

Typical Performance Characteristics (cont.)

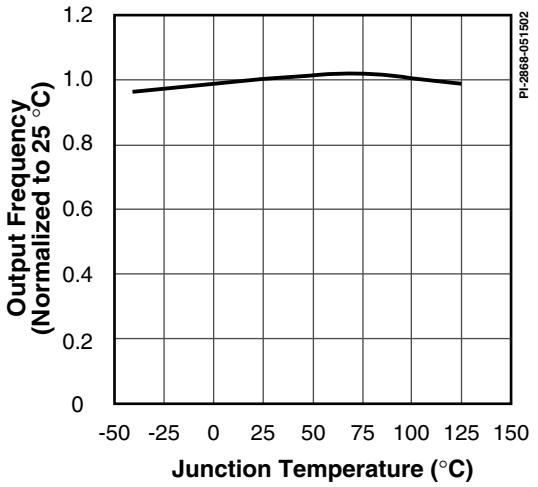


Figure 36. Frequency vs. Temperature.

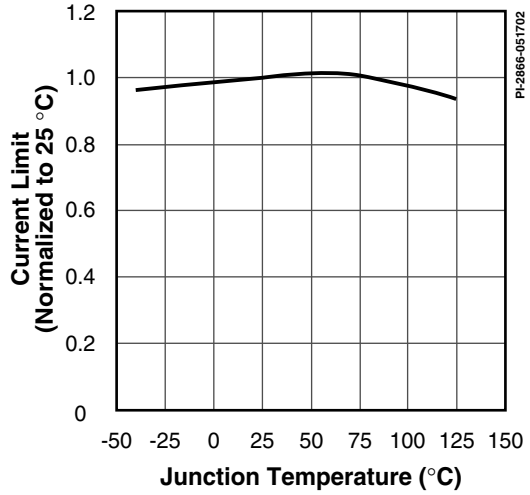


Figure 37. Internal Current Limit vs. Temperature.

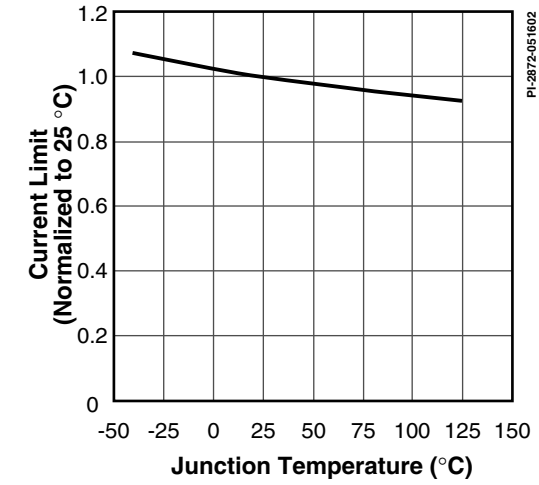


Figure 38. External Current Limit vs. Temperature with R_{IL} = 12 kΩ.

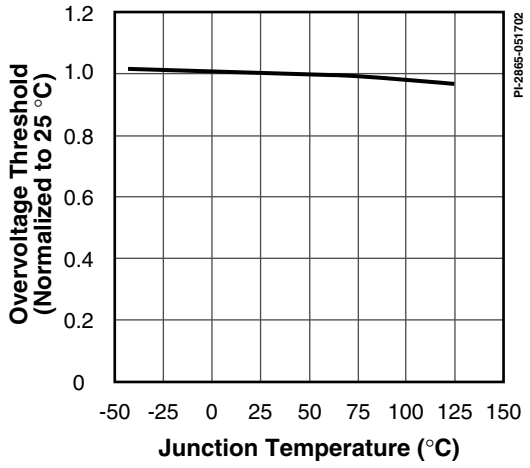


Figure 39. Overvoltage Threshold vs. Temperature.

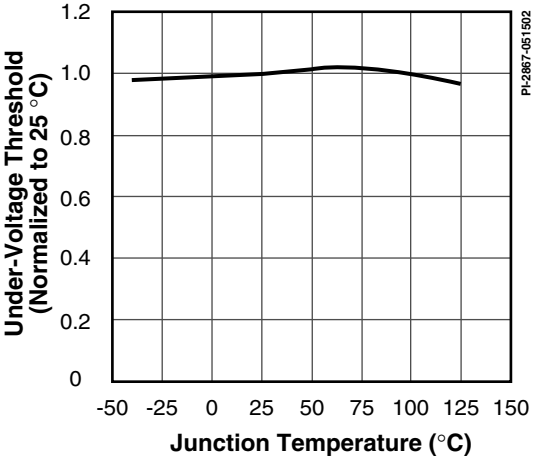


Figure 40. Under-Voltage Threshold vs. Temperature.

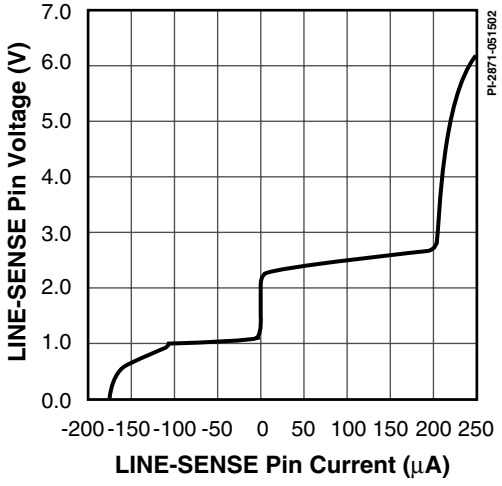


Figure 41. LINE-SENSE Pin Voltage vs. Current.

Typical Performance Characteristics (cont.)

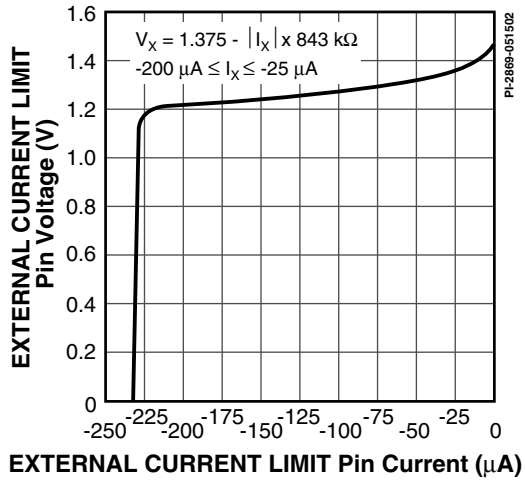


Figure 42. EXTERNAL CURRENT LIMIT Pin Voltage vs. Current

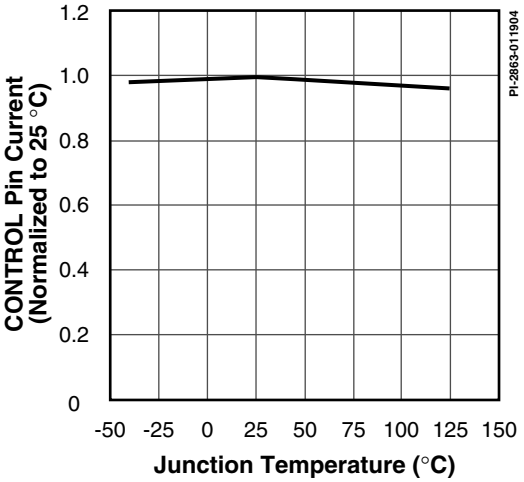


Figure 43. CONTROL Pin Current at Minimum Duty Cycle vs. Temperature.

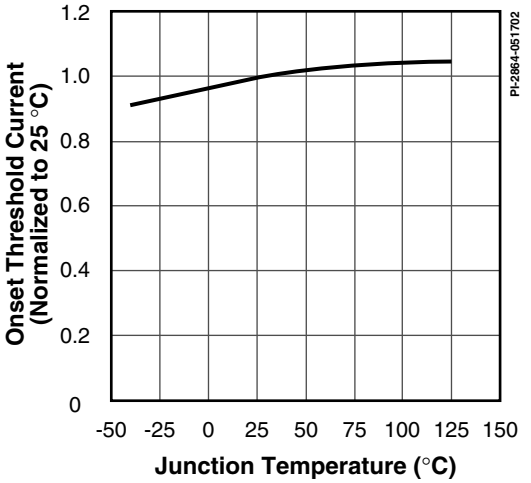


Figure 44. Max. Duty Cycle Reduction Onset Threshold Current vs. Temperature.

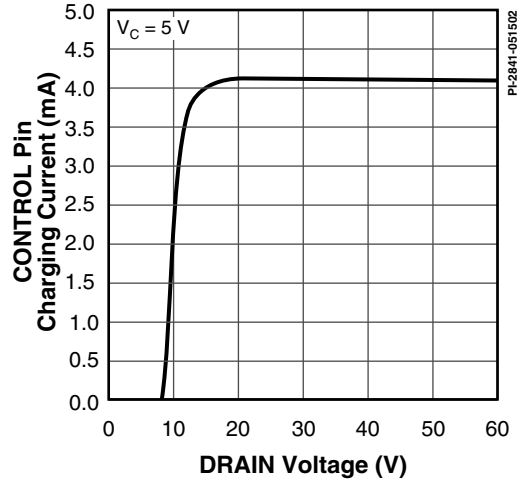


Figure 45. I_C vs. DRAIN Voltage.

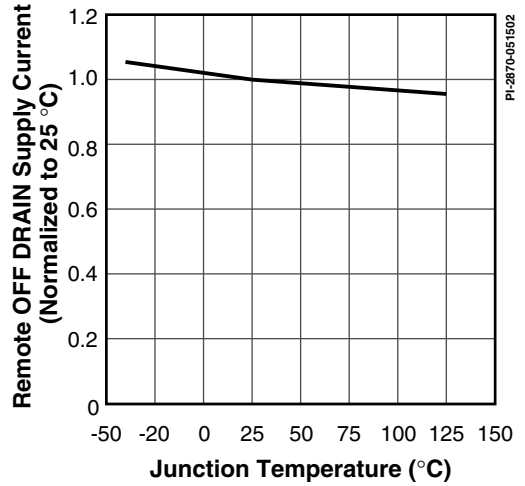


Figure 46. Remote OFF DRAIN Supply Current vs. Temperature.

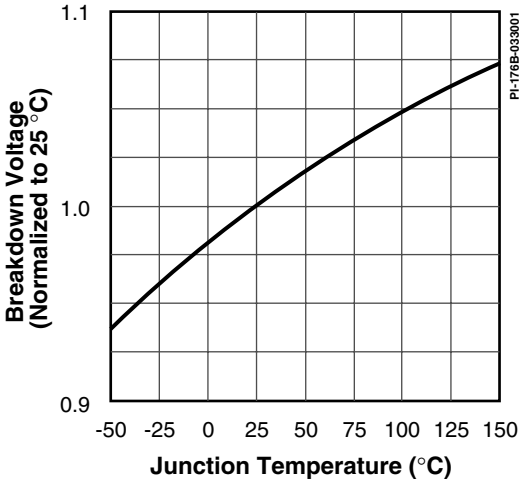


Figure 47. Breakdown Voltage vs. Temperature.

Typical Performance Characteristics (cont.)

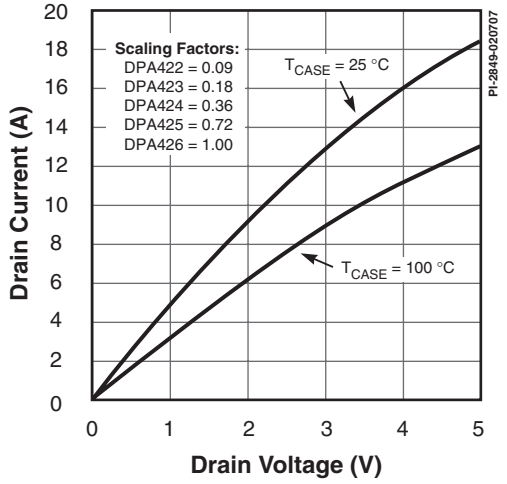


Figure 48. Output Characteristics.

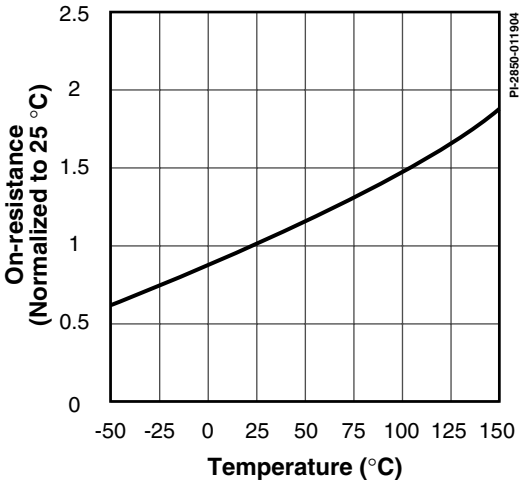


Figure 49. On-Resistance vs. Temperature.

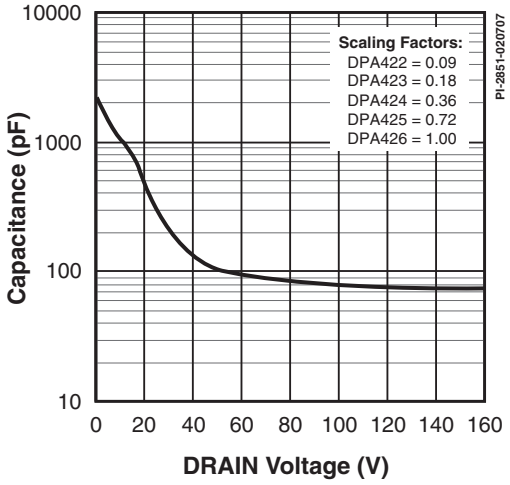


Figure 50. C_{oss} vs. DRAIN Voltage.

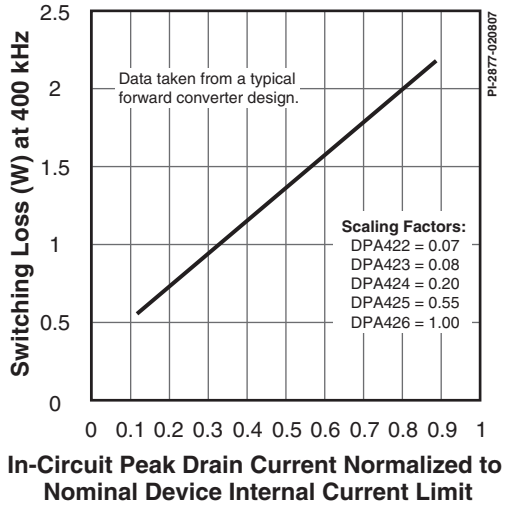


Figure 51. Typical Switching Loss.

PART ORDERING INFORMATION

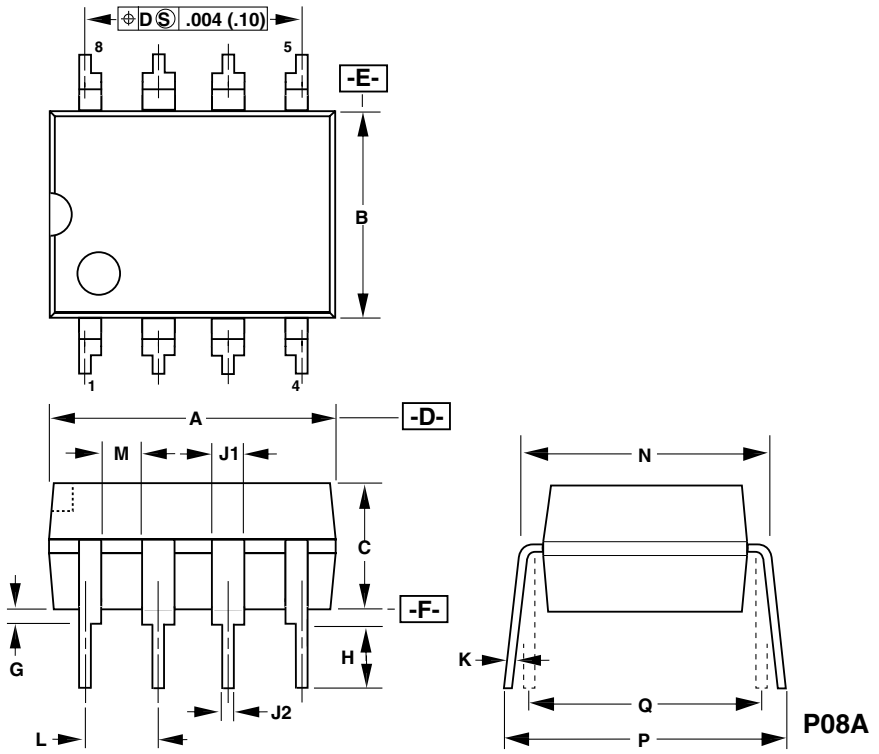
DPA 423 G N - TL

***DPA-Switch* Product Family**		
Series Number		
Package Identifier		
G	Plastic Surface Mount DIP	(422, 423, 424 & 425 only)
P	Plastic DIP	
R	Plastic TO-263-7C (available only with TL option)	
S	S-PAK (available only with TL option)	(423, 424, 425 & 426 only)
Lead Finish		
Blank	Standard (Sn Pb) not available with S-PAK	
N	Pure Matte Tin (Pb-Free) (P & G packages and S-PAK)	
Tape & Reel and Other Options		
Blank	Standard Configurations	
TL	Tape & Reel, (G package and S-PAK: 1000 min./mult., R package: 750 min./mult.)	

DIP-8

DIM	inches	mm
A	0.367-0.387	9.32-9.83
B	0.240-0.260	6.10-6.60
C	0.125-0.145	3.18-3.68
G	0.015-0.040	0.38-1.02
H	0.120-0.140	3.05-3.56
J1	0.057-0.068	1.45-1.73
J2	0.014-0.022	0.36-0.56
K	0.008-0.015	0.20-0.38
L	0.100 BSC	2.54 BSC
M	0.030 (MIN)	0.76 (MIN)
N	0.300-0.320	7.62-8.13
P	0.300-0.390	7.62-9.91
Q	0.300 BSC	7.62 BSC

Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85).
2. Controlling dimensions are inches.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. D, E and F are reference datums on the molded body.



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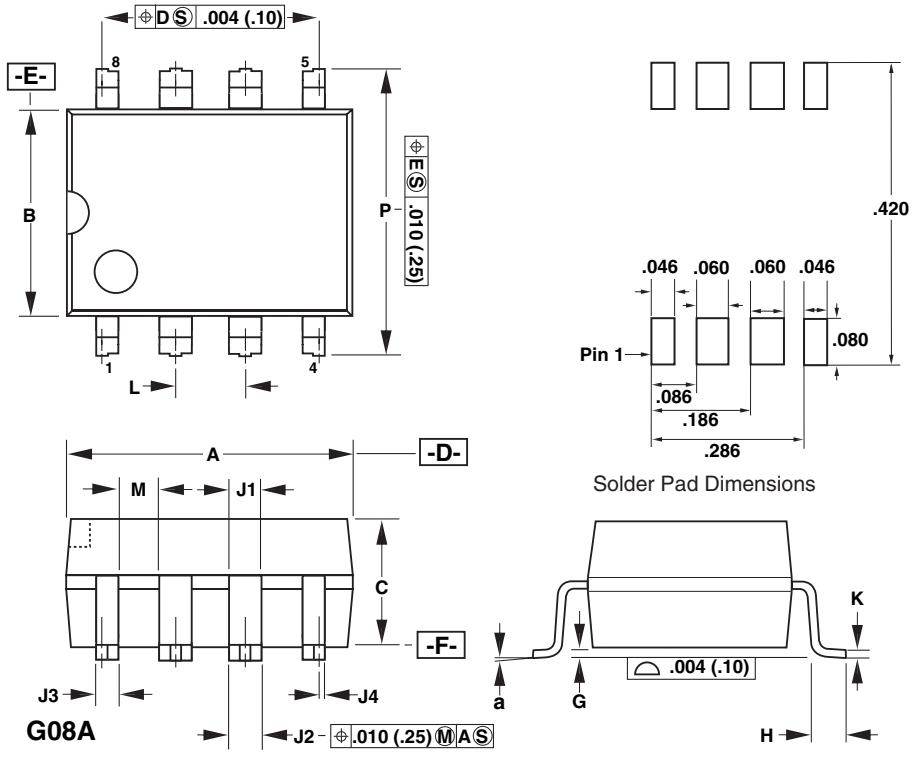
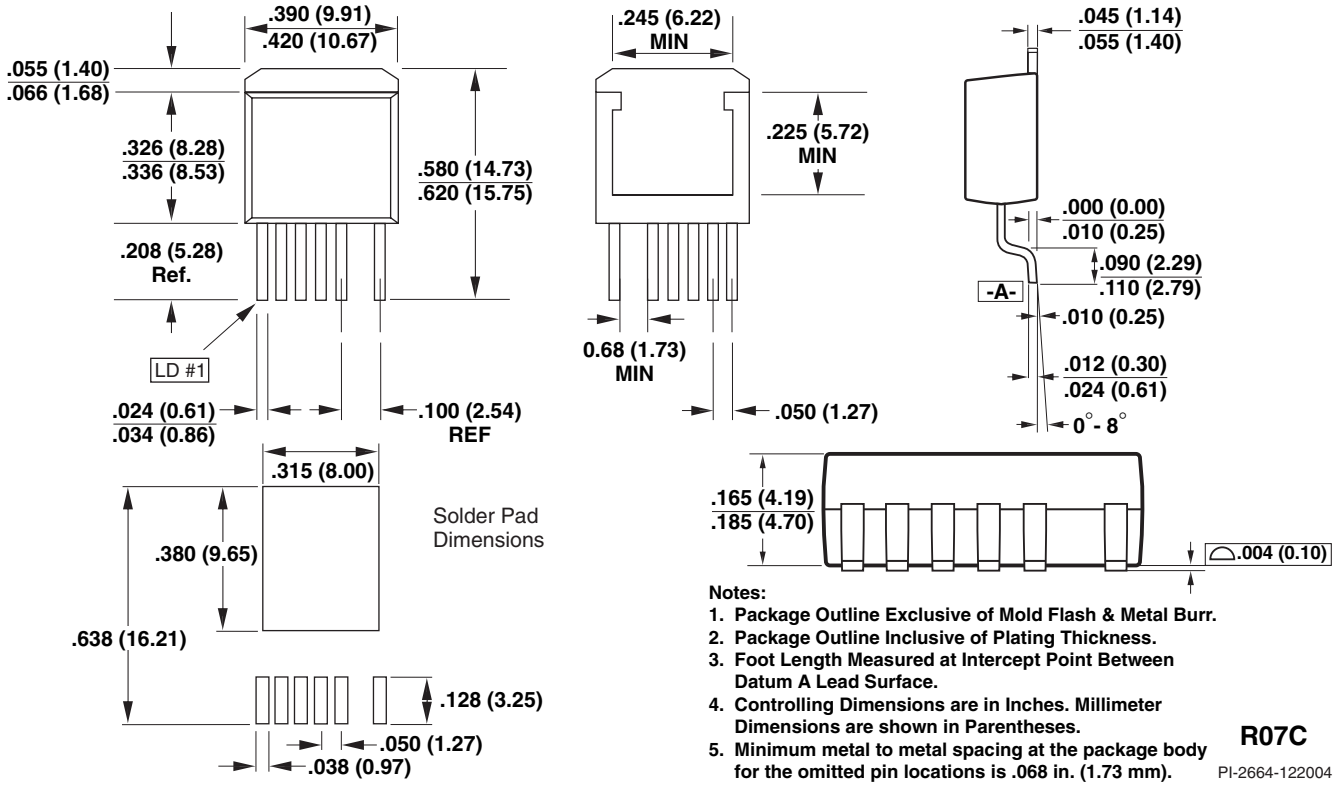


DIM	inches	mm
A	0.367-0.387	9.32-9.83
B	0.240-0.260	6.10-6.60
C	0.125-0.145	3.18-3.68
G	0.004-0.012	0.10-0.30
H	0.036-0.044	0.91-1.12
J1	0.057-0.068	1.45-1.73
J2	0.048-0.053	1.22-1.35
J3	0.032-0.037	0.81-0.94
J4	0.007-0.011	0.18-0.28
K	0.010-0.012	0.25-0.30
L	0.100 BSC	2.54 BSC
M	0.030 (MIN)	0.76 (MIN)
P	0.372-0.388	9.45-9.86
a	0-8°	0-8°

Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB (issue B, 7/85) except for lead shape and size.
2. Controlling dimensions are inches.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. D, E and F are reference datums on the molded body.

PI-2077-041003

TO-263-7C



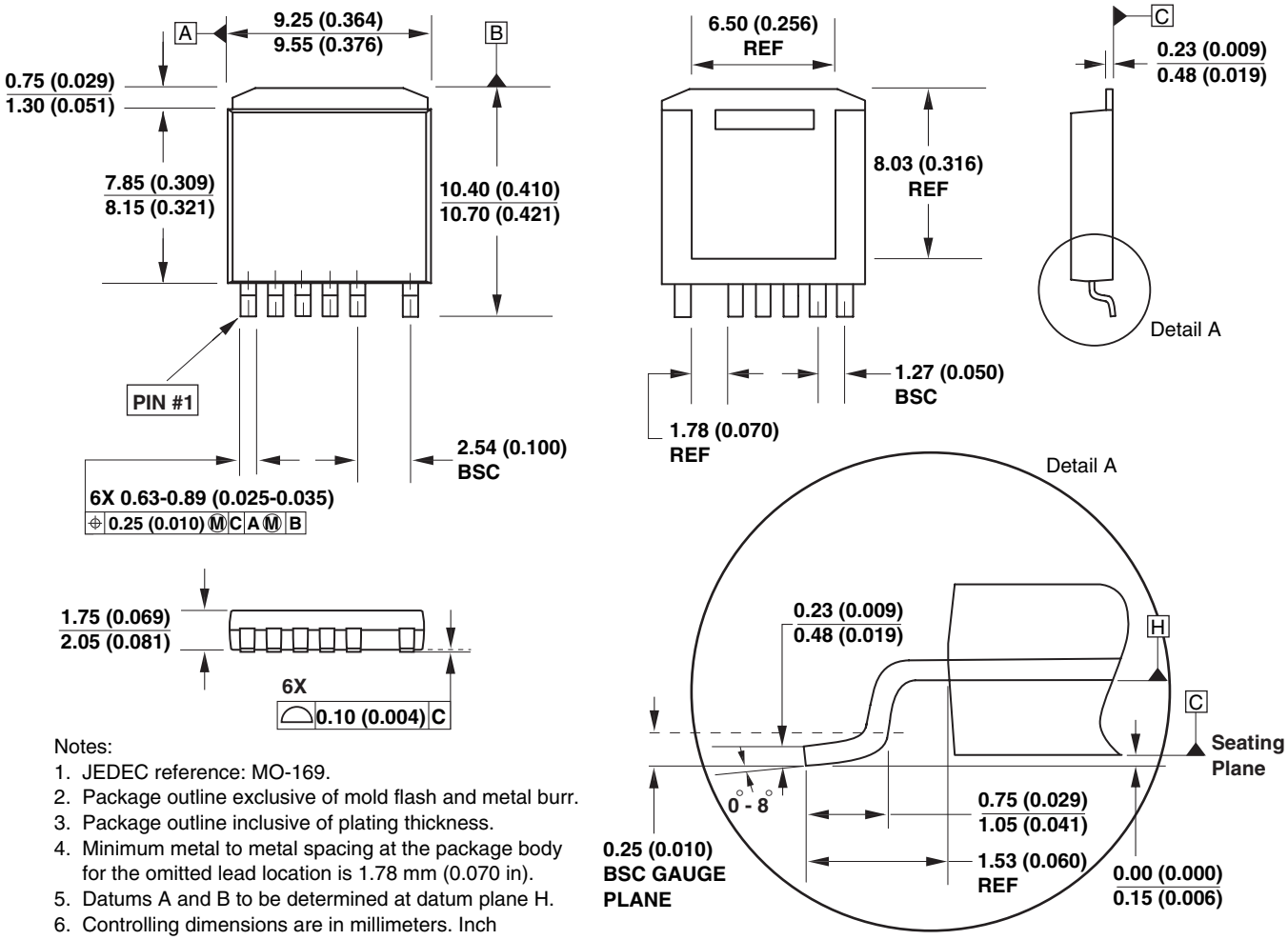
Notes:

1. **Package Outline Exclusive of Mold Flash & Metal Burr.**
2. **Package Outline Inclusive of Plating Thickness.**
3. **Foot Length Measured at Intercept Point Between Datum A Lead Surface.**
4. **Controlling Dimensions are in Inches. Millimeter Dimensions are shown in Parentheses.**
5. **Minimum metal to metal spacing at the package body for the omitted pin locations is .068 in. (1.73 mm).**

R07C

PI-2664-122004

S-PAK MO-169-7C

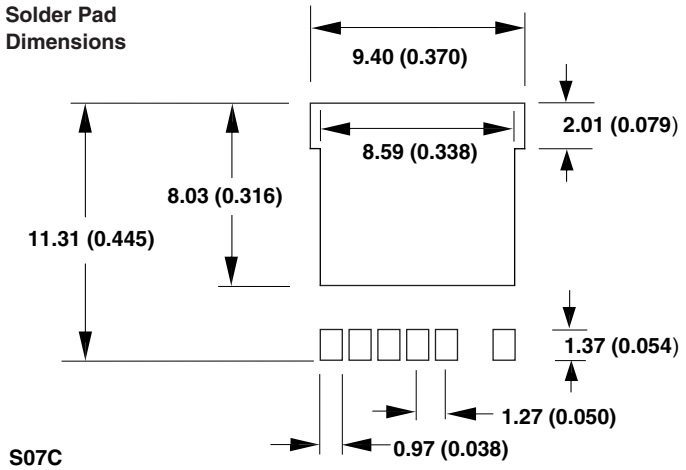


Notes:
1. JEDEC reference: MO-169.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Minimum metal to metal spacing at the package body for the omitted lead location is 1.78 mm (0.070 in).
5. Datums A and B to be determined at datum plane H.
6. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis.

S07C

PI-4024-071405

Solder Pad Information For S-PAK



S07C

PI-4034-071405

Revision	Notes	Date
F	Final release data sheet.	6/02
G	Updated Figure 25 and text description.	9/02
H	Corrected missing text on page 9 and corrected Table 4. Updated R package description. Revised thermal impedances (θ_{JA}), DC_{MIN}, V_F, I_F, and BV_{DSS}. Updated Figure 25 and description in text.	4/03
I	Corrected text errors on pp. 1, 7 and 20.	5/03
J	Figure 25 and description in text updated.	5/03
K	Added P and G packages.	1/04
L	Corrected Figure 3.	4/04
M	Added package information to Table 1. Revised Figure 13. Added lead-free ordering information.	12/04
N	Minor error corrections.	2/05
O	Added S-PAK.	7/05
P	Added notes to Table 6.	7/05
Q	Updated Figure 27 to best reflect current requirements for PoE.	5/06
R	Added DPA422.	2/07

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