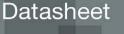


LVDS Interface ICs **27bit LVDS Transmitter** BU90T81





General Description

The BU90T81 transmitter operates from 20MHz to 112MHz wide clock range, and 27bits data of parallel LVCMOS level inputs(R/G/B24bits and VSYNC,HSYNC,DE) are converted to four channels of LVDS data stream. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less.

The BU90T81 operates from a single 1.8V supply for low power. And the BU90T81 has low swing mode to be able to expect further low power and low EMI

Features

- ■24bits data of parallel LVCMOS level inputs are converted to four channels of LVDS data stream.
- ■Support clock frequency from 20MHz up to 112MHz.
- ■Low power 1.8V CMOS design
- ■Power down mode
- ■Clock edge selectable
- ■Support 6bit/8bit mode selectable
- ■Support reduced swing LVDS for low EMI.
- Support LVDS Outputs pin reverse function
- ■Support spread spectrum clock generator input

Block Diagram

•Key Specifications

- Supply Voltage range
- Operating frequencyOperating Temperature Range
- Power Consumption

20 to 112MHz -20 to 85°C 50mW(Typ)

4.00 mm × 4.00 mm × 0.90 mm

1.65 to 1.95 V

Packages

VBGA048W040

Applications

- Tablet
- Netbook PC
- Digital Picture Frame

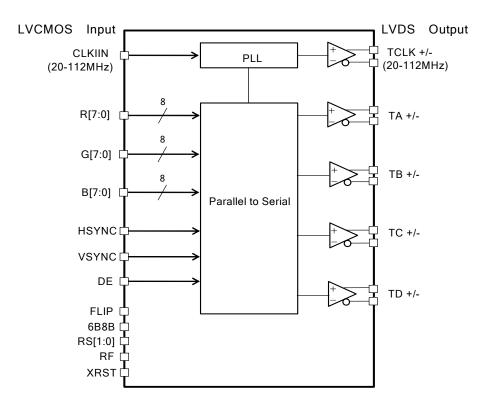


Figure-1 Block Diagram

OProduct structure : Silicon monolithic integrated circuit oThis product is not designed protection against radioactive rays

Pin Configuration

Top view

	1	2	3	4	5	6	7
A	G[5]	G[7]	R[1]	R[3]	R[5]	R[6]	R[7]
в	I	G[6]	R[0]	R[2]	R[4]	TA-	TA+
С	G[3]	G[4]	GND	RS[1]	RS[0]	TB-	TB+
D	G[1]	G[2]	RF	VDD	VDD	TC-	TC+
E	G[0]	B[7]	FLIP	6B8B	GND	TCLK-	TCLK+
F	B[6]	B[5]	B[2]	B[0]	DE	TD-	TD+
G	B[4]	B[3]	B[1]	HSYNC	VSYNC	CLKIN	XRST

48pin VBGA

Figure-2 Pin Diagram (Top View)

Pin Description

Pin Name	Pin No.	Туре	Descriptions	
TA+/-, TB+/-, TC+/-,TD+/-	B7,B6,C7,C6,D7,D6,F7,F6	LVDS	LVDS Data out	
TCLK+/-	E7,6	OUT	LVDS Clock out	
R[7:0]	A7,A6,A5,B5,A4,B4,A3,B3			
G[7:0]	A2,B2,A1,C2,C1,D2,D1,E1		Pixel and control data inputs	
B[7:0]	E2,F1,F2,G1,G2,F3,G3,F4	CMOS		
HSYNC,VSYNC, DE	G4,G5,F5	IN		
CLKIN	G6		Clock input	
XRST	G7		Power Down H : Normal operation L : Power down (all LVDS output signal are Hi-z)	
RF	D3		Input CLK Triggering Edge Select. H:Rising edge L:Falling edge	
RS[1:0]	C3,C5	CMOS IN	LVDS swing mode selectRS1RS0LVDS swingLLTYP=160mVLHTYP=200mVHLTYP=350mVHHReserved	
6B8B	E4		6bit/8bit mode select H : 6bit mode(FLIP=L TD+/- is Hiz) (FLIP=H TA+/- is Hiz) L : 8bit mode	
FLIP	E3		LVDS output pin reverse select. H : Reverse L : Normal	
VDD	D4,D5	POWER	1.8V Power supply	
GND	C3,E5	GND	Ground Pins	

Absolute Maximum Ratings

Parameter	Symbol	Rat	Units	
Farameter	Symbol	Min	Max	Units
Supply Voltage	V _{DD}	-0.3	2.5	V
Input Voltage	V _{IN}	-0.3	V _{DD} +0.3	V
Output Voltage	V _{OUT}	-0.3	V _{DD} +0.3	V
Storage Temperature Range	Tstg	-55	125	°C

Operating Ratings

	Symbol	Rating			Units	Conditions
Parameter	Symbol	Min	Тур	Max	01113	Conditions
Supply Voltage	V _{DD}	1.65	1.8	1.95	V	
Operating Temperature Range	Topr	-20	-	85	°C	
Operating frequency	Fmax	20	-	112	MHz	

Package Power

Package	Power Dissipation (mW)	De-rating (mW/°C)*1
VBGA048W040	800*1	8.0*1

*1:Package power when mounting on the PCB board.

The size of PCB board The material of PCB board

: 114.3×76.2×1.6(mm³)

B board : The FR4 glass epoxy board.

•DC characteristics

Table 1 : LVCMOS DC Specifications (V_{DD}=1.65V~1.95V, Ta=-20°C~+85°C)

Symbol	Parameter	Rating			Units	Conditions	
Symbol	Falameter	Min	Тур	Max	Units	Conditions	
VIH	High Level Input Voltage	$V_{DD} \times 0.7$	-	V _{DD}	V		
V _{IL}	Low Level Input Voltage	GND	-	$V_{DD} \times 0.3$	V		
I _{INC}	Input Current	-10	-	+10	μA	0V≤V _{IN} ≤V _{DD}	

Table2: LVDS Transmitter DC Specifications (V_{DD}=1.65V~1.95V, Ta=-20°C~+85°C)

Symbol	Parameter	Rating			Units	Conditions	
Symbol	Farameter	Min	Тур	Max	Units	Conditions	
		250	350	450	mV		RS[1:0]= HL
V _{OD}	Differential Output Voltage	130	200	270	mV	RL=100Ω	RS[1:0]= LH
		110	160	210	mV		RS[1:0]= LL
ΔV_{OD}	Change in VOD between complementary output states	-	-	35	mV		
Voc	Common Mode Voltage	1.125	1.25	1.375	V	RL=100Ω	
ΔV _{OC}	Change in VOC between complementary output states	-	-	35	mV		
los	Output Short Circuit Current	-90	-	-	mA	V _{OUT} =0V	
l _{oz}	Output TRI-STATE Current	-10	-	+10	μA	XRST=0V, V _{OUT} =0V to V	DD

AC characteristics

		_		
Table 3 · Switching	g Characteristics(VDD=1.8V	/ Ta-25℃	RI -1000	$CI = 5rr E R S[1 \cdot 0] = HI$
	y Onalaciensilos (V D D – 1.0 V	, 1a-20 0	IXE-10032	

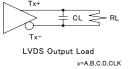
Symbol	Param	neter	Min	Тур	Max	Units
t _{TCP}	CLK OUT	Period	8.93	-	50	ns
tтсіт	CLK IN Tran	sition time	-	-	5.0	ns
t _{TCH}	CLK IN Hi	gh Time	0.35t _{TCP}	0.5t _{TCP}	0.65t _{TCP}	ns
t _{TCL}	CLK IN L	ow Time	$0.35t_{\text{TCP}}$	0.5t _{TCP}	0.65t _{TCP}	ns
t _{TS}	LVSMOS Data S	et up to CLK IN	2.5	-	-	ns
tтн	LVCMOS Data He	old from CLK IN	0	-	-	ns
t _{LVT}	LVDS Trans	ition Time	-	0.6	1.5	ns
T _{TSUP}	Differential Output Set up Time	CLKOUT=112MHz	-	-	200	pS
T _{THLD}	Differential Output Hold time	CLKOUT=112MHz	-	-	200	pS
t _{TOP6}	Output Data	Position 6	$2\frac{\text{ttcp}}{7}$ - T _{THLD}	2 tтср 7	$2\frac{\text{ttcp}}{7} + \text{T}_{\text{TSUP}}$	ns
t _{TOP5}	Output Data	Position 5	$3\frac{\text{ttcp}}{7}$ - T _{THLD}	3 tтср 7	$3\frac{\text{trcp}}{7}$ + T _{TSUP}	ns
t _{TOP4}	Output Data	Position 4	$4\frac{\text{ttcp}}{7}$ - T _{THLD}	4 tтср 7	$4\frac{\text{trcp}}{7}$ + T _{TSUP}	ns
t _{TOP3}	Output Data	Position 3	$5\frac{\text{ttcp}}{7}$ - T _{THLD}	5 1 TCP 7	$5\frac{\text{ttcp}}{7} + \text{T}_{\text{TSUP}}$	ns
t _{TOP2}	Output Data	$6\frac{\text{ttcp}}{7}$ - T _{THLD}	6 tтср 7	$6\frac{\text{ttcp}}{7} + \text{T}_{\text{TSUP}}$	ns	
t _{TOP1}	Output Data	$7\frac{tTCP}{7} - T_{THLD}$	7 tтср 7	$7\frac{\text{trcp}}{7} + \text{T}_{\text{TSUP}}$	ns	
t _{TOP0}	Output Data	Position 0	$8\frac{\text{ttcp}}{7}$ - T _{THLD}	8 tтср 7	$8\frac{\text{ttcp}}{7}$ + T _{TSUP}	ns
t _{TPLL}	Phase Locked L	oop Set Time	-	-	10	ms

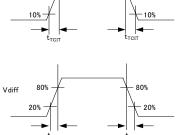
●AC Timing Diagrams

LVCMOS Input

LVDS Output



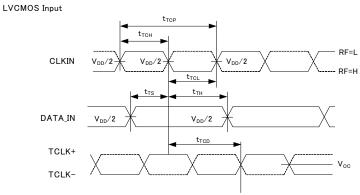




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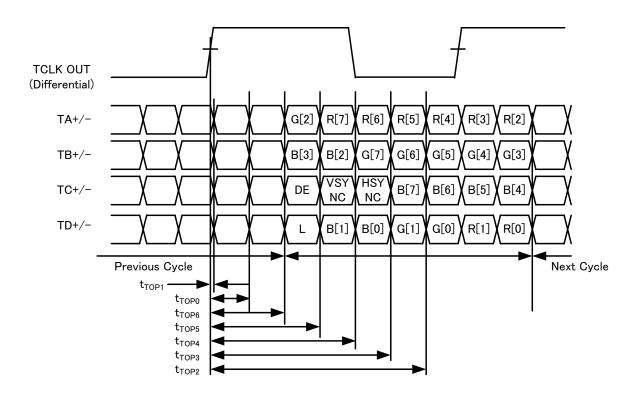
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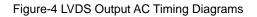
CLKIN



DATA_IN= R[7:0], G[7:0], B[7:0], VSYNC, HSYNC, DE

Figure-3 LVCMOS Input AC Timing Diagrams





Phase Locked Loop Set Time

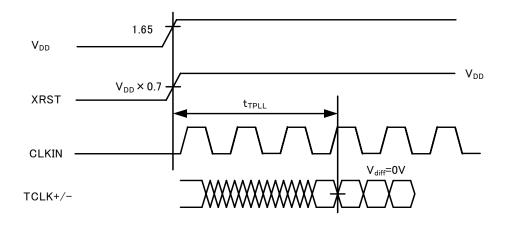


Figure-5 Phase Locked Loop Set Time

Supply Current

Table 4: Supply Current (6B8B = L)

Symbol	Deremeter	•	Rating		Units	Conditions		
Symbol	Parameter	Min	Тур	Max	Units	Conditions		
		-	30.4	-	mA	RL=100Ω,CL=5pF VDD=1.8V,RS[1:0]=HL Gray Scale Pattern f=85MHz		
I _{TCCG}	Transmitter Supply Current	-	22.5	-	mA	RL=100Ω,CL=5pF VDD=1.8V,RS[1:0]=LH Gray Scale Pattern f=85MHz		
		-	20.4	-	mA	RL=100Ω,CL=5pF VDD=1.8V, RS[1:0]=LL Gray Scale Pattern		
	Transmitter Supply Current	-	32.4	-	mA	RL=100Ω,CL=5pF VDD=1.8V, RS[1:0]=HL Worst case Pattern		
I _{TCCW}		-	24.5	-	mA	RL=100Ω,CL=5pF VDD=1.8V, RS[1:0]=LH Worst case Pattern		
		-	22.4	-	mA	RL=100Ω,CL=5pF VDD=1.8V, RS[1:0]=LL Worst case Pattern		
I _{TCCS}	Transmitter Power Down Supply Current	-	-	10	μA	XRST=L		

Gray Scale Pattern

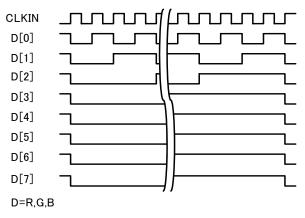
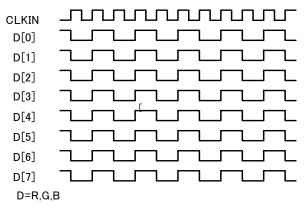
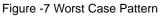


Figure -6 Gray Scale Pattern

Worst Case Pattern (Maximum Power condition)

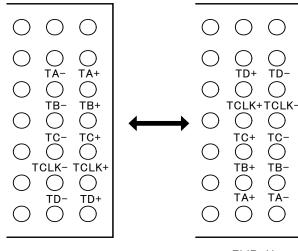




●LVDS Data Output Table for Function of FLIP pin

Table 5: LVDS Data Output Pin Nam	е
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	Output Pin Names					
Pin No	FLIP=L	FLIP=H				
B7	TA+	TD-				
B6	TA-	TD+				
C7	TB+	TCLK-				
C6	TB-	TCLK+				
D7	TC+	TC-				
D6	TC-	TC+				
E7	TCLK+	TB-				
E6	TCLK-	TB+				
F7	TD+	TA-				
F6	TD-	TA+				



FLIP=L

FLIP=H

•LVCMOS Data Inputs Pixel Map Table

Table 6: LVCMOS Data Inputs Pixel Map Table

	TFT Panel Da			
	24Bit	18Bit	BU90T81 Input	
LSB	R0	-	R0	
	R1	-	R0	
	R2	R0	R1	
	R3	R1	R2	
	R4	R2	R3	
	R5	R3	R4	
	R6	R4	R5	
MSB	R7	R5	R6	
LSB	G0	-	R7	
	G1	-	G0	
	G2	G0	G1	
	G3	G1	G2	
	G4	G2	G3	
	G5	G3	G4	
	G6	G4	G5	
MSB	G7	G5	G6	
LSB	B0	-	G7	
	B1	-	B0	
	B2	B0	B1	
	B3	B1	B2	
	B4	B2	B3	
	B5	B3	B4	
	B6	B4	B5	
MSB	B7	B5	B6	
	VSYNC	VSYNC	B7	
	HSYNC	HSYNC	HSYNC	
	DE	DE	DE	

LVDS Output Data Mapping

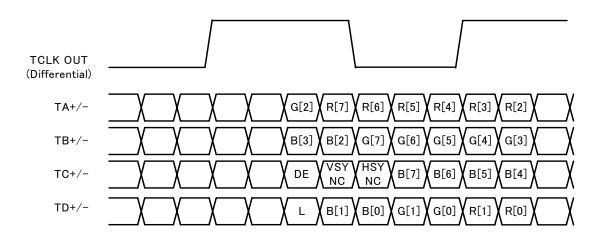


Figure-8 LVDS output mapping (6B8B=L, FLIP=L)

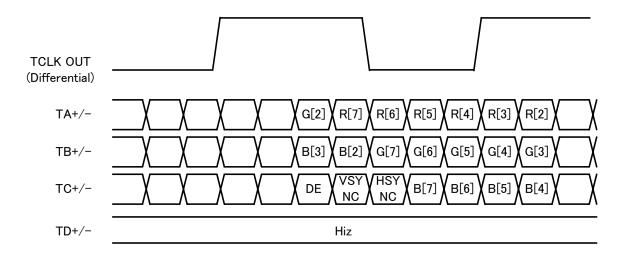


Figure-9 LVDS output mapping (6B8B=H, FLIP=L)

•Typical Application Circuit (24bit mode)

Example

BU90T81: LVCMOS Data Input /rising edge/200mV swing output/normal output mapping

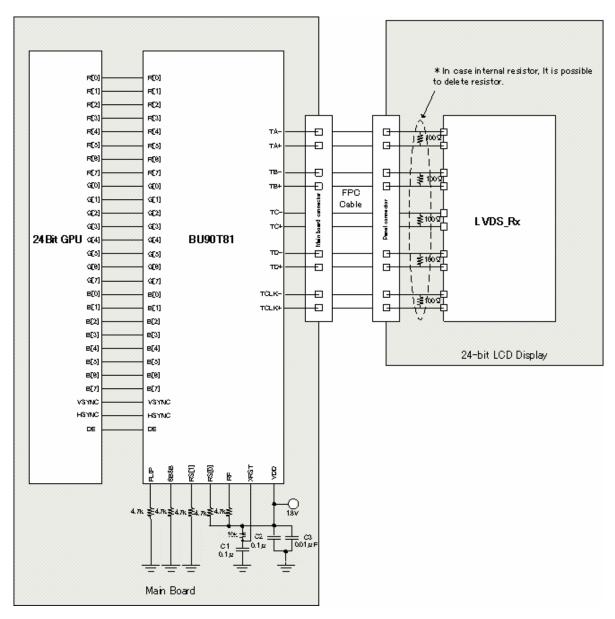


Figure-10 Application Circuit (24bit mode)

•Typical Application Circuit (18bit mode)

Example

BU90T81: LVCMOS Data Input /rising edge/200mV swing output/normal output mapping

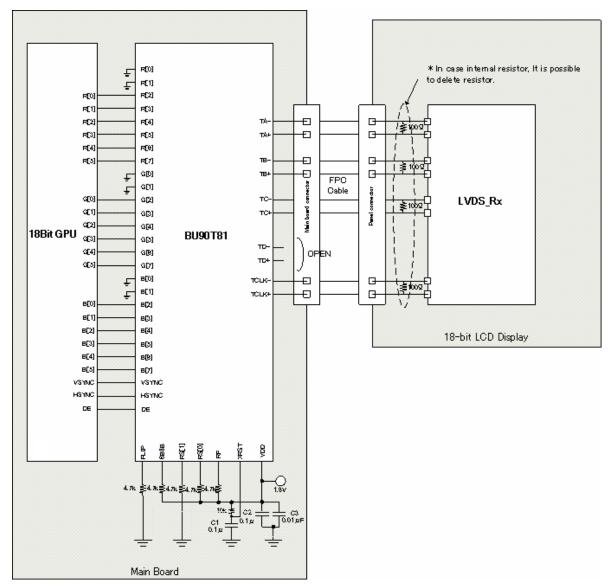


Figure-11 Application Circuit (18bit mode)

Status of this document

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