

FDMS86101DC

POWERTRENCH[®] MOSFET, N-Channel, DUAL COOL[®] 56 Shielded Gate

100 V, 60 A, 7.5 mΩ

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced POWERTRENCH[®] process that incorporates Shielded Gate technology. Advancements in both silicon and DUAL COOL[®] package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Features

- Shielded Gate MOSFET Technology
- DUAL COOL Top Side Cooling PQFN package
- Max $r_{DS(on)}$ = 7.5 mΩ at $V_{GS} = 10$ V, $I_D = 14.5$ A
- Max $r_{DS(on)}$ = 12 mΩ at $V_{GS} = 6$ V, $I_D = 11.5$ A
- High performance technology for extremely low $r_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

Typical Applications

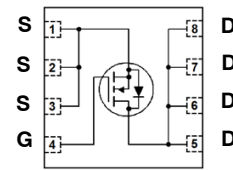
- Primary DC-DC MOSFET
- Secondary Synchronous Rectifier
- Load Switch



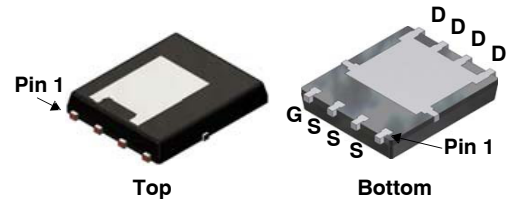
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ELECTRICAL CONNECTION

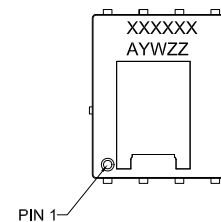


N-Channel MOSFET



DFN8 5.1x6.15
(Dual Cool 56)
CASE 506EG

MARKING DIAGRAM



XXXXXX	= Device Code
A	= Assy Location
Y	= Year Code
WW	= Work Week Code
ZZ	= Assy Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMS86101DC

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping†
86101	FDMS86101DC	UDFN8	13"	12 mm	3000 Units/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Units
V _{DS}	Drain to Source Voltage	100	V
V _{GS}	Gate to Source Voltage	±20	V
I _D	Drain Current –Continuous T _C = 25°C	60	A
	–Continuous T _A = 25°C (Note 1a)	14.5	
	–Pulsed	200	
E _{AS}	Single Pulse Avalanche Energy (Note 3)	216	mJ
P _D	Power Dissipation T _C = 25°C	125	W
	Power Dissipation T _A = 25°C (Note 1a)	3.2	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		70		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 44 μA	2	2.7	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		–10		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 14.5 A		6	7.5	mΩ
		V _{GS} = 4.5 V, I _D = 11.5 A		8.3	12	
		V _{GS} = 10 V, I _D = 14.5 A, T _J = 125°C		10	13	
g _{FS}	Forward Transconductance	V _{DD} = 10 V, I _D = 14.5 A		44		S

DYNAMIC CHARACTERISTICS

C _{ISS}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		2354	3135	pF
C _{OSS}	Output Capacitance			467	625	pF
C _{RSS}	Reverse Transfer Capacitance			23	35	pF
R _G	Gate Resistance			0.1	1.4	3

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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SWITCHING CHARACTERISTICS

t _{d(ON)}	Turn – On Delay Time	V _{DD} = 50 V, I _D = 14.5 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		14	25	ns
t _r	Rise Time			8.2	17	ns
t _{D(OFF)}	Turn – Off Delay Time			25	40	ns
t _f	Fall Time			5.5	11	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V V _{GS} = 0 V to 5 V		31	44	nC
	Total Gate Charge			18	25	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 50 V, I _D = 14.5 A		8.3		nC
Q _{gd}	Gate to Drain "Miller" Charge			7		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.7 A (Note 2)		0.71	1.2	V
		V _{GS} = 0 V, I _S = 14.5 A (Note 2)		0.78	1.3	
t _{rr}	Reverse Recovery Time	I _F = 14.5 A, di/dt = 100 A/μs		54	87	ns
Q _{rr}	Reverse Recovery Charge			62	99	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

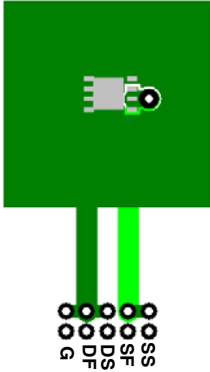
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Units
R _{θJC}	Thermal Resistance, Junction to Case (Top Source)	2.3	°C/W
R _{θJC}	Thermal Resistance, Junction to Case (Bottom Drain)	1.0	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	38	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1b)	81	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1c)	27	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1d)	34	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1e)	16	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1f)	19	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1g)	26	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1h)	61	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1i)	16	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1j)	23	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1k)	11	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1l)	13	

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NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 38°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 81°C/W when mounted on a minimum pad of 2 oz copper.

- c) Still air, 20.9×10.4×12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- d) Still air, 20.9×10.4×12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e) Still air, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- f) Still air, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g) .200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
- h) .200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i) .200FPM Airflow, 20.9×10.4×12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- j) .200FPM Airflow, 20.9×10.4×12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k) .200FPM Airflow, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- l) .200FPM Airflow, 45.2×41.4×11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting $T_J = 25^\circ\text{C}$; N-ch: $L = 0.3\text{ mH}$, $I_{AS} = 38\text{ A}$, $V_{DD} = 90\text{ V}$, $V_{GS} = 10\text{ V}$.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

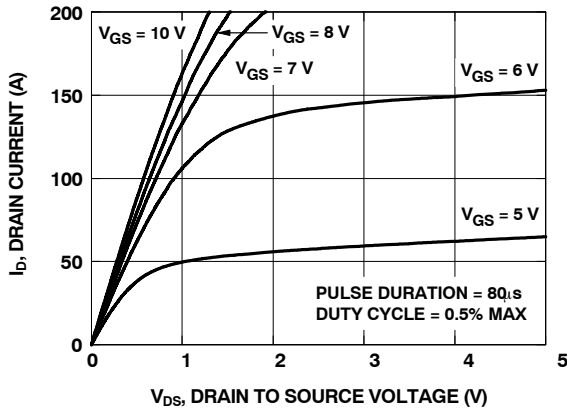


Figure 1. On Region Characteristics

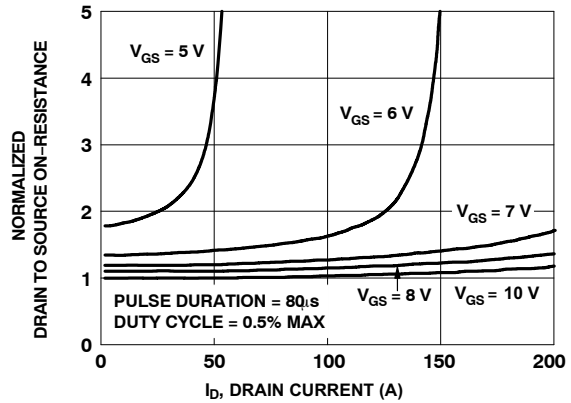


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

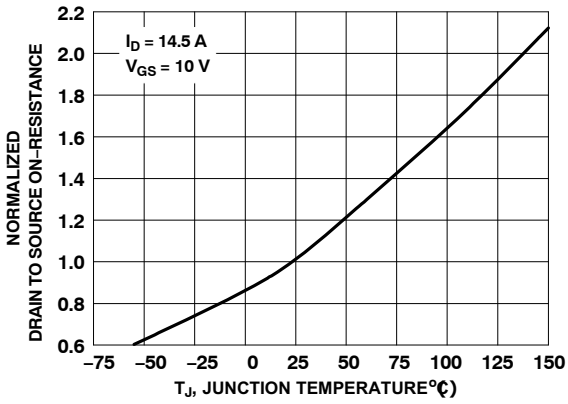


Figure 3. Normalized On Resistance vs. Junction Temperature

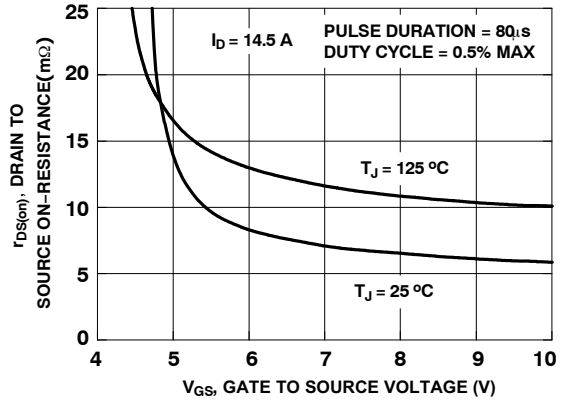


Figure 4. On-Resistance vs. Gate to Source Voltage

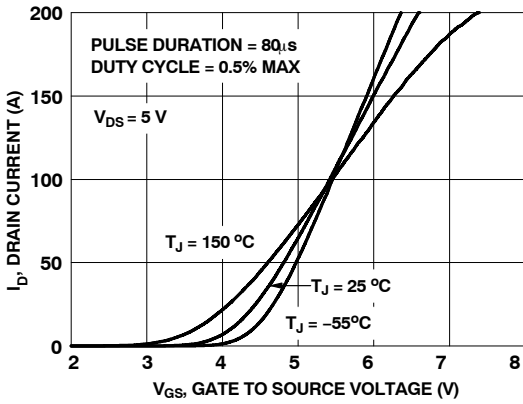


Figure 5. Transfer Characteristics

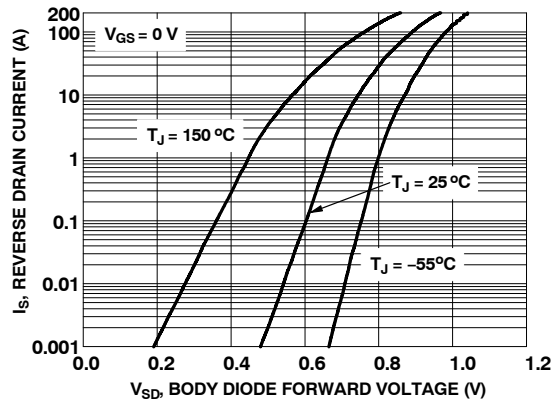


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

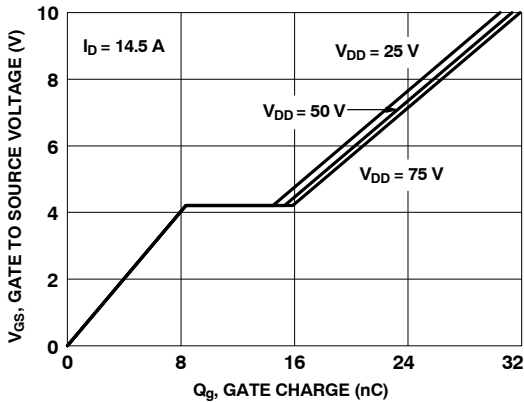


Figure 7. Gate Charge Characteristics

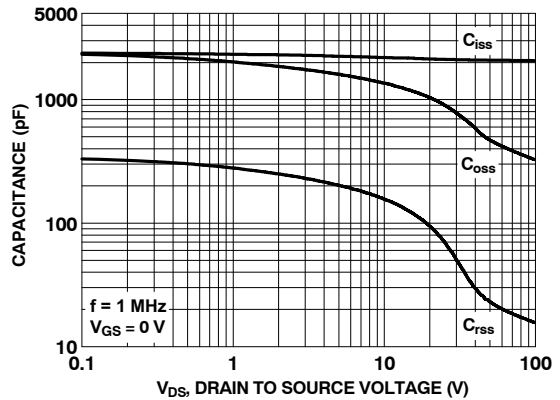


Figure 8. Capacitance vs. Drain to Source Voltage

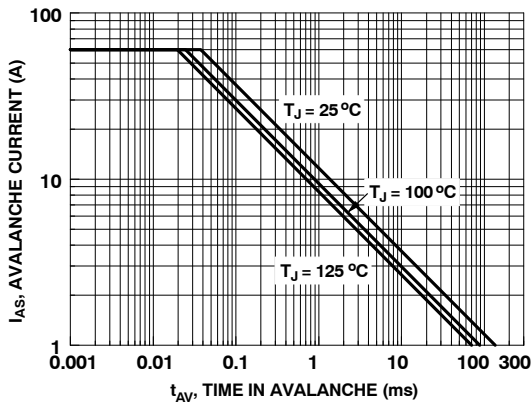


Figure 9. Unclamped Inductive Switching Capability

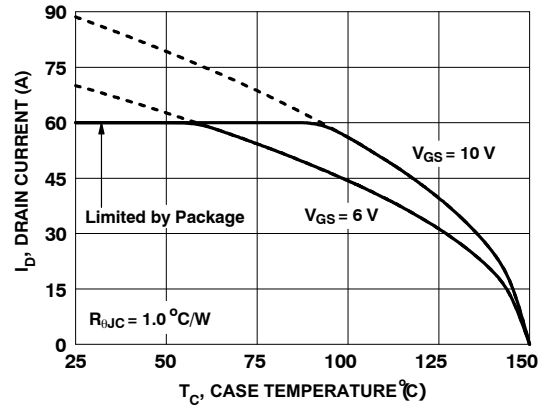


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

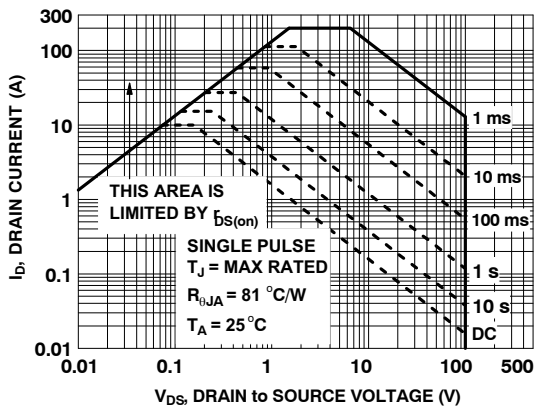


Figure 11. Forward Bias Safe Operating Area

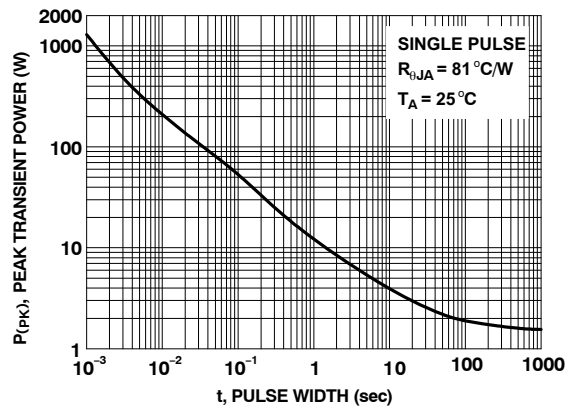


Figure 12. Single Pulse Maximum Power Dissipation

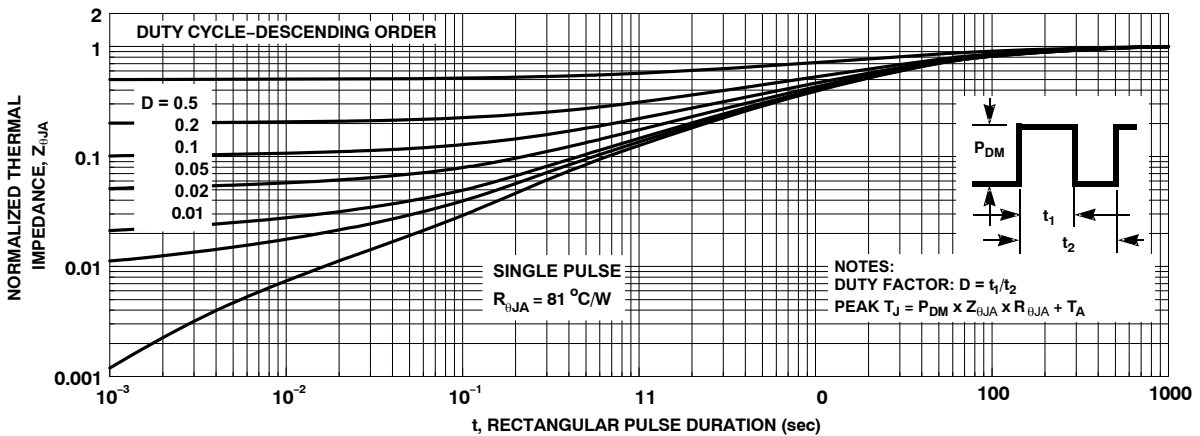


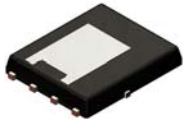
Figure 13. Junction-to-Case Transient Thermal Response Curve

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MECHANICAL CASE OUTLINE

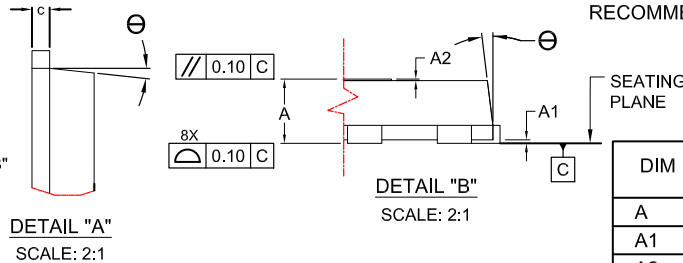
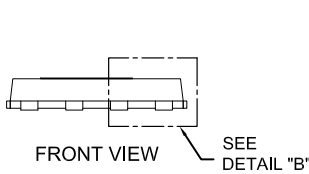
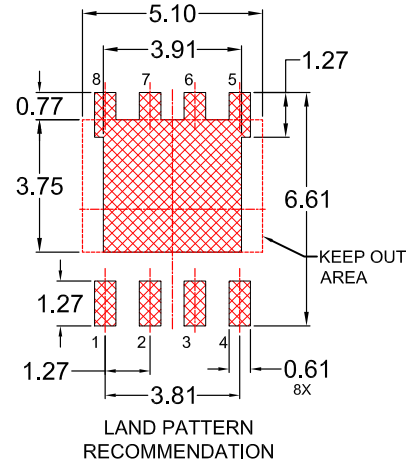
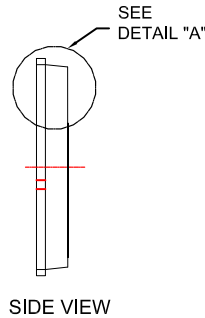
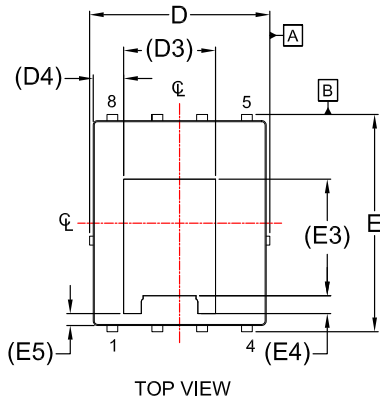
PACKAGE DIMENSIONS

ON Semiconductor®

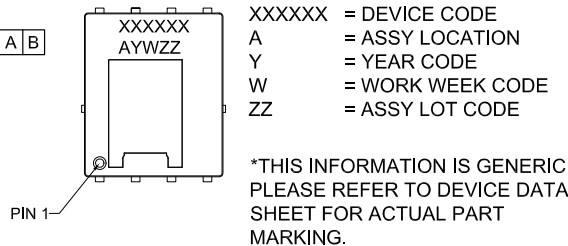
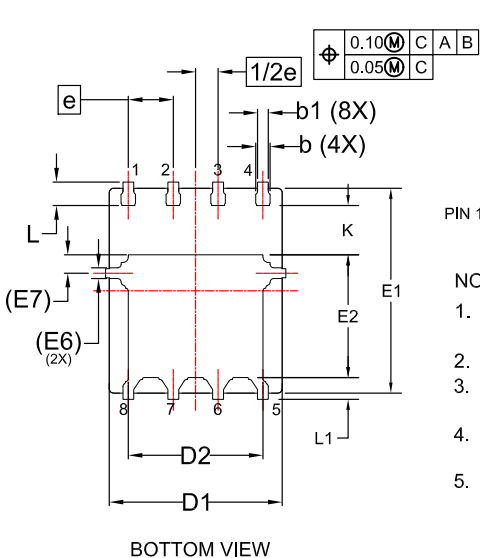


DFN8 5.1x6.15, 1.27P
CASE 506EG
ISSUE A

DATE 18 JUL 2018



GENERIC MARKING DIAGRAM



XXXXXX = DEVICE CODE
 A = ASSY LOCATION
 Y = YEAR CODE
 W = WORK WEEK CODE
 ZZ = ASSY LOT CODE

*THIS INFORMATION IS GENERIC.
 PLEASE REFER TO DEVICE DATA SHEET FOR ACTUAL PART MARKING.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
θ	0°	--	12°

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